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NEC LCD Technologies, Ltd.

TFT COLOR LCD MODULE

NL3224BC35-22

14cm (5.5 Type)
QVGA

DATA SHEET

DOD-PP-0301 (6th edition)

This DATA SHEET is updated document from DOD-PP-0065(5).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL3224BC35-22 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing circuit, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- For industrial use

1.3 FEATURES

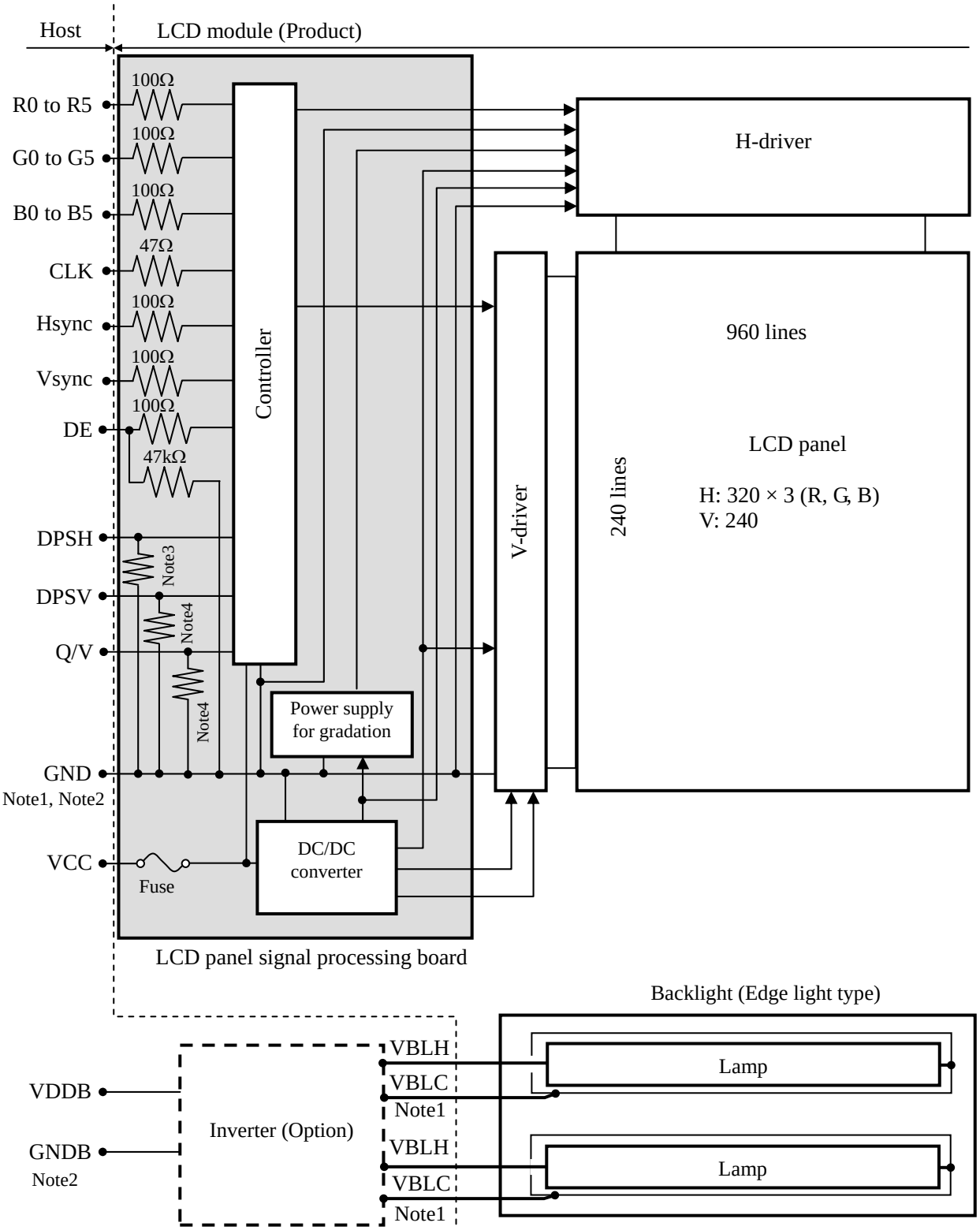
- Adoption of ST-NLT (Super-Transmissive Natural Light TFT)
- High luminance
- Wide color gamut
- Wide viewing angle
- Low reflection
- 6-bit digital RGB signals
- Reversible-scan direction
- Selectable QVGA or VGA mode
- Edge light type (without inverter)
- Replaceable lamp for backlight
- Acquisition product for UL60950-1/CSA-C22.2 No.60950-1-03 (File number: E170632)
- Compliance with the European RoHS directive (2002/95/EC) ☆
  (From product which was produced after April. 1, 2006)

2. GENERAL SPECIFICATIONS

Display area	111.36 (H) × 83.52 (V) mm
Diagonal size of display	14cm (5.5 inches)
Drive system	a-Si TFT active matrix
Display color	262,144 colors
Pixel	320 (H) × 240 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Dot pitch	0.116 (H) × 0.348 (V) mm
Pixel pitch	0.348 (H) × 0.348 (V) mm
Module size	134.0 (W) × 104.5 (H) × 12.5 (D) mm (typ.)
Weight	215g (typ.)
Contrast ratio Note1	500:1 (typ.)
Viewing angle Note1	*At the contrast ratio≥ 10:1* • Horizontal: Right side 55° (typ.), Left side 55° (typ.) • Vertical: Up side 50° (typ.), Down side 40° (typ.)
Designed viewing direction	*At DPSH, DPSV= Low or Open: Normal scan* • Viewing direction without image reversal: down side (6 o'clock) • Viewing direction with contrast peak: up side (12 o'clock) • Viewing angle with optimum grayscale (γ=2.2): normal axis (perpendicular)
Polarizer surface	Clear + Antireflection (AR)
Polarizer pencil-hardness	2H (min.) [by JIS K5400]
Color gamut	*At LCD panel center* 50% (typ.) [against NTSC color space]
Response time	*Ton+Toff (10%←→90%)* 30ms (typ.)
Luminance	*At IBL= 5.0mArms / lamp* 750cd/m^2 (typ.)
Signal system	6-bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE), Horizontal synchronous signal (Hsync), Vertical synchronous signal (Vsync)
Power supply voltage	LCD panel signal processing board: 3.3V or 5.0V
Backlight	Edge light type: 2 cold cathode fluorescent lamps (Replaceable part • Lamp holder set: Type No. 55LHS11) (Recommended inverter (Option) • Inverter: Type No. 55PW131)
Power consumption Note1	*At IBL=5.0mArms / lamp, Checkered flag pattern* 3.8W (typ., Power dissipation of the inverter is not included.)

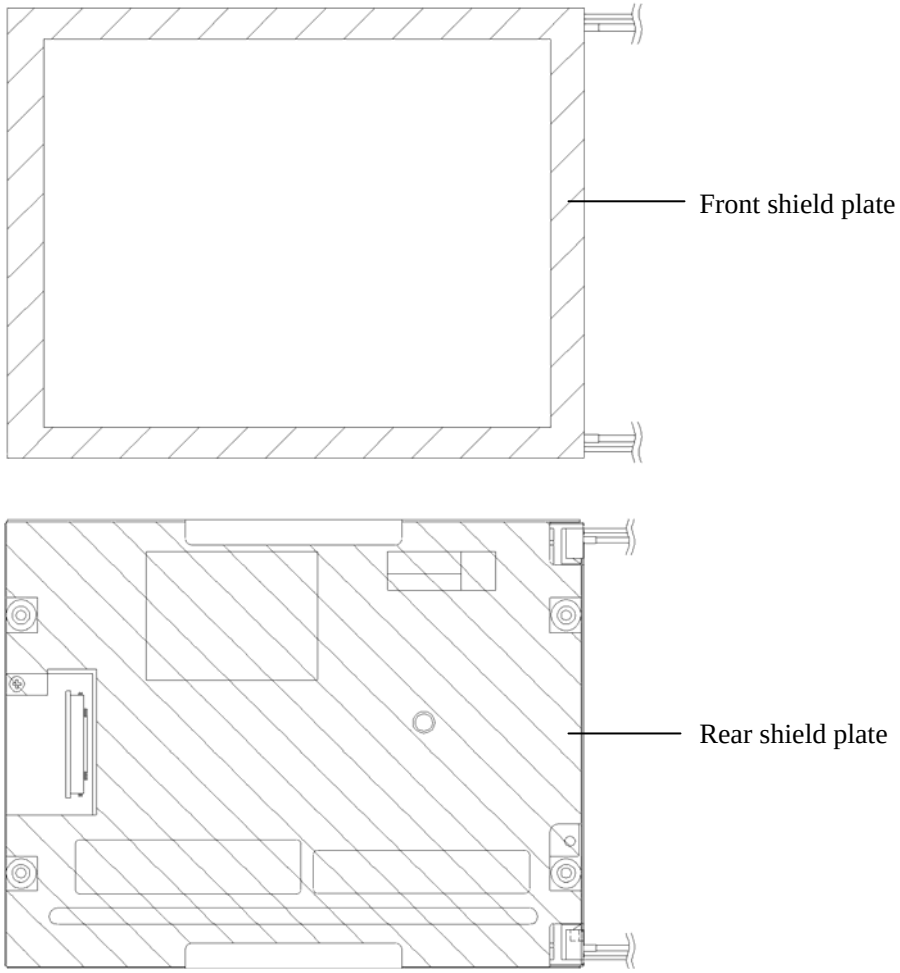
Note1: At QVGA mode

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), shield plate and VBLC (Lamp low voltage terminal) in the LCD module are as follows.

Front shield plate - Rear shield plate	Not connected
GND - Front shield plate and Rear shield plate	Not connected
VBLC - Front shield plate and Rear shield plate	Not connected
GND - VBLC	Not connected



Note2: GND and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds are connected together in customer equipment.

Note3: Pull-down resistance of DPSH pin

Power supply voltage VCC	Pull-down resistance of DPSH pin (kΩ)		
	min.	typ.	max.
at 3.3V	8.2	13.0	18.3
at 5.0V	6.0	10.0	15.0

Note4: Pull-down resistance of DPSV pin and Q/V pin

Power supply voltage VCC	Pull-down resistance of DPSV pin and Q/V pin (kΩ)		
	min.	typ.	max.
at 3.3V	13.0	18.3	23.0
at 5.0V	10.0	15.0	20.0

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	134.0 ± 0.5 (W) × 104.5 ± 0.5 (H) × 12.5 ± 0.5 (D) Note1	mm
Display area	111.36 (H) × 83.52 (V) Note1	mm
Weight	215 (typ.), 225 (max.)	g

Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VCC	-0.3 to +6.5	V	Ta= 25°C
	Lamp voltage	VBLH	1,500	Vrms	
Input voltage for signals	Display signals Note1	VD	-0.3 to VCC+0.3	V	
	Function signals Note2	VF			
Incident light intensity		II	150,000	lx	Note3
Storage temperature		Tst	-30 to +80	°C	-
Operating temperature	Front surface	TopF	-10 to +70	°C	Note4
	Rear surface	TopR	-10 to +75	°C	Note5
Relative humidity Note6		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40 < Ta ≤ 50°C
			≤ 70	%	50 < Ta ≤ 55°C
			≤ 60	%	55 < Ta ≤ 60°C
			≤ 50	%	60 < Ta ≤ 65°C
			≤ 42	%	65 < Ta ≤ 70°C
Absolute humidity Note6		AH	≤ 83 Note7	g/m^3	Ta > 70°C

Note1: CLK, Hsync, Vsync, DE, DATA (R0 to R5, G0 to G5, B0 to B5)
Note2: DPSH, DPSV, Q/V
Note3: If the product surface (polarizer) is exposed to an ultraviolet ray, the polarizer may discolor (Surface treatment may be damaged.). Use a filter to protect the polarizer from the ultraviolet ray.
Note4: Measured at center of LCD panel surface (including self-heat)
Note5: Measured at center of LCD module's rear shield surface (including self-heat)
Note6: No condensation
Note7: Water amount at Ta= 70°C and RH= 42%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VCC	3.0	3.3	3.6	V	at VCC= 3.3V
			4.75	5.0	5.25	V	at VCC= 5.0V
Power supply current	QVGA mode	ICC	-	65 Note1	105 Note2	mA	at VCC= 3.3V
			-	50 Note1	85 Note2	mA	at VCC= 5.0V
	VGA mode		-	95 Note1	175 Note2	mA	at VCC= 3.3V
			-	70 Note1	130 Note2	mA	at VCC= 5.0V
Logic input voltage for display signals	High	VDLH	0.7VCC	-	VCC	V	CMOS level
	Low	VDLL	0	-	0.3VCC	V	
Input voltage for DPSH, DPSV and Q/V signal	High	VFDH	0.7VCC	-	VCC	V	-
	Low	VFDL	0	-	0.9	V	

Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: Pattern for maximum current

4.3.2 Backlight lamp

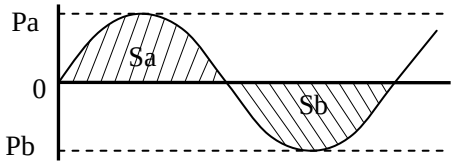
(Ta=25°C, Note1)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current Note3	IBL	4.5	5.0	5.5	mArms	at IBL= 5.0mArms: L= 750cd/m^2
Lamp voltage Note2, Note3	VBLH	-	350	-	Vrms	-
Lamp starting voltage Note2, Note3, Note4, Note7	VS	550	-	-	Vrms	Ta= 25°C
		780	-	-	Vrms	Ta= -10°C
Lamp oscillation frequency Note5	FO	39	43	47	kHz	-

Note1: This product consists of 2 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal). When designing the inverter, evaluate asymmetric of lamp working waveform sufficiently.



$$\frac{|Pa - Pb|}{Pb} \times 100 \leq 5\ \%$$

$$\frac{|Sa - Sb|}{Sb} \times 100 \leq 5\ \%$$

Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part.

Note4: The inverter should be designed so that the lamp starting voltage can be maintained for more than 1 second. Otherwise the lamp may not be turned on.

Note5: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following

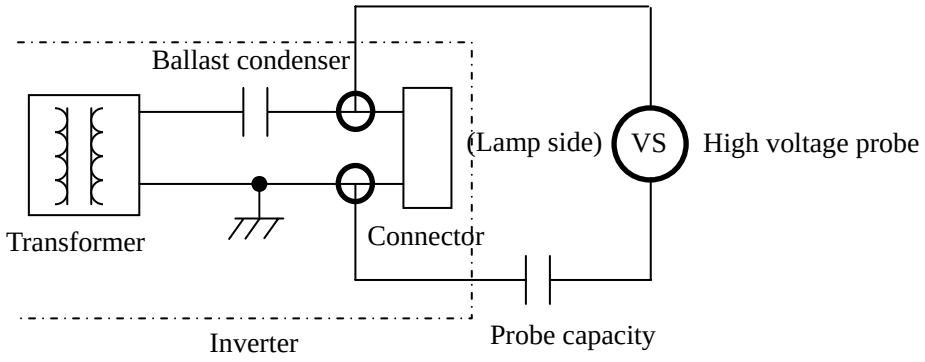
$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle (See "**4.9 INPUT SIGNAL TIMINGS**".)
n: Natural number (1, 2, 3 ·····)

Note6: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.

Note7: In case of Inverter with Ballast condenser, "VS" is the voltage level between Ballast condenser and Connector (Refer to the below “Example of measurement”). "VS" should be designed to be more than minimum "VS". Otherwise the lamp may not be turned on because the lamp starting voltage is less than minimum "VS". ☆

Example of measurement
Probe capacity: 3pF (Tektronix, inc.: P6015A)



4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VCC	3.3V	≤ 100	mVp-p
	5.0V	≤ 100	mVp-p

Note1: The permissible ripple voltage includes spike noise.

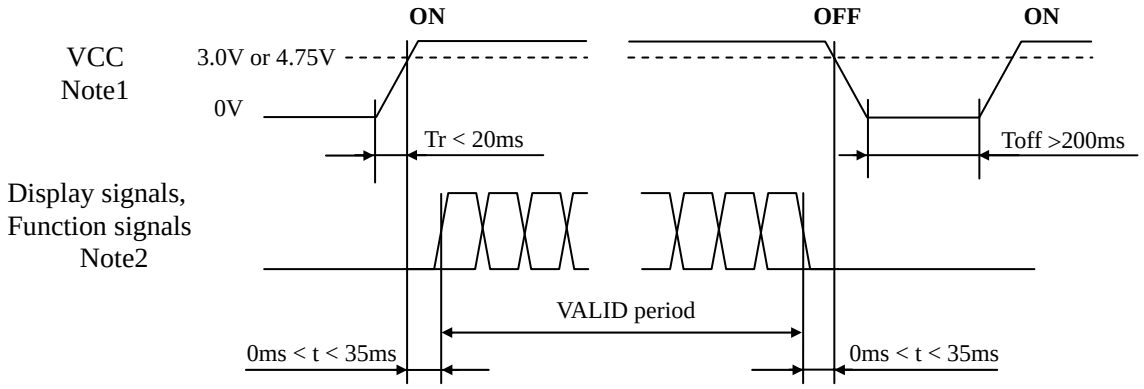
4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VCC	ICP-S1.8	ROHM Co., Ltd.	1.8A 50V	4.0A	Note1

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

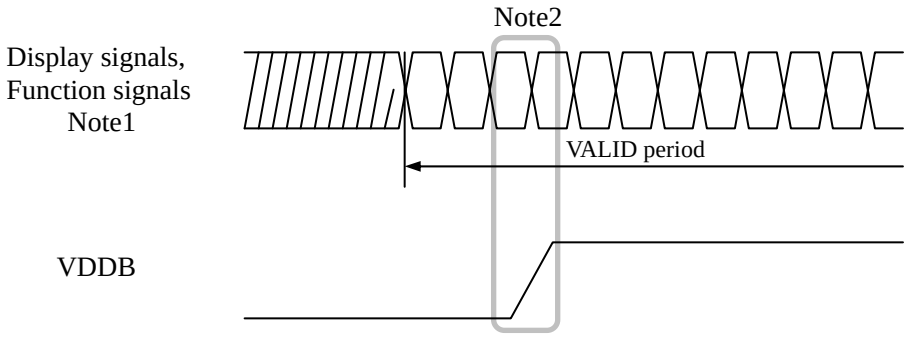
4.4.1 LCD panel signal processing board



Note1: In terms of voltage variation (voltage drop) while VCC rising edge is below 3.0V in "VCC = 3.3V" or 4.75V in "VCC = 5.0V", a protection circuit may work, and then this product may not work.

Note2: Display signals (CLK, Hsync, Vsync, DE, DATA (R0 to R5, G0 to G5, B0 to B5)) and function signals (DPSH, DPSV, Q/V) must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.
If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. VCC should be cut when the display and function signals are stopped.

4.4.2 Inverter (Option)



Note1: These are the display and function signals for LCD panel signal processing board.

Note2: The backlight should be turned on within the valid period of display and function signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): 08 6260 033 340 829+ (Kyocera Elco Corp.)

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	CLK	Dot clock	-
3	Hsync	Horizontal synchronous signal	
4	Vsync	Vertical synchronous signal	
5	GND	Ground	Note1
6	R0	Red data (LSB)	Least significant bit
7	R1	Red data	-
8	R2	Red data	
9	R3	Red data	
10	R4	Red data	
11	R5	Red data (MSB)	Most significant bit
12	GND	Ground	Note1
13	G0	Green data (LSB)	Least significant bit
14	G1	Green data	-
15	G2	Green data	
16	G3	Green data	
17	G4	Green data	
18	G5	Green data (MSB)	Most significant bit
19	GND	Ground	Note1
20	B0	Blue data (LSB)	Least significant bit
21	B1	Blue data	-
22	B2	Blue data	
23	B3	Blue data	
24	B4	Blue data	
25	B5	Blue data (MSB)	Most significant bit
26	GND	Ground	Note1
27	DE	Selection of DE / Fixed mode	Data enable signal: DE mode High or Open: Fixed mode
28	VCC	Power supply	Note1
29	VCC	Power supply	
30	DPSH	Selection of scan direction (Horizontal)	Low or Open: Normal scan High: Reverse scan Note2
31	DPSV	Selection of scan direction (Vertical)	
32	Q/V	Selection of QVGA / VGA mode	High: VGA mode Low or Open: QVGA mode Note2
33	GND	Ground	Note1

Note1: All VCC and GND terminals should be used without any non-connected lines.
Note2: See "**4.8 SCANNING DIRECTIONS**".

4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. Wrong connections will cause electric shock and also break down of the product.

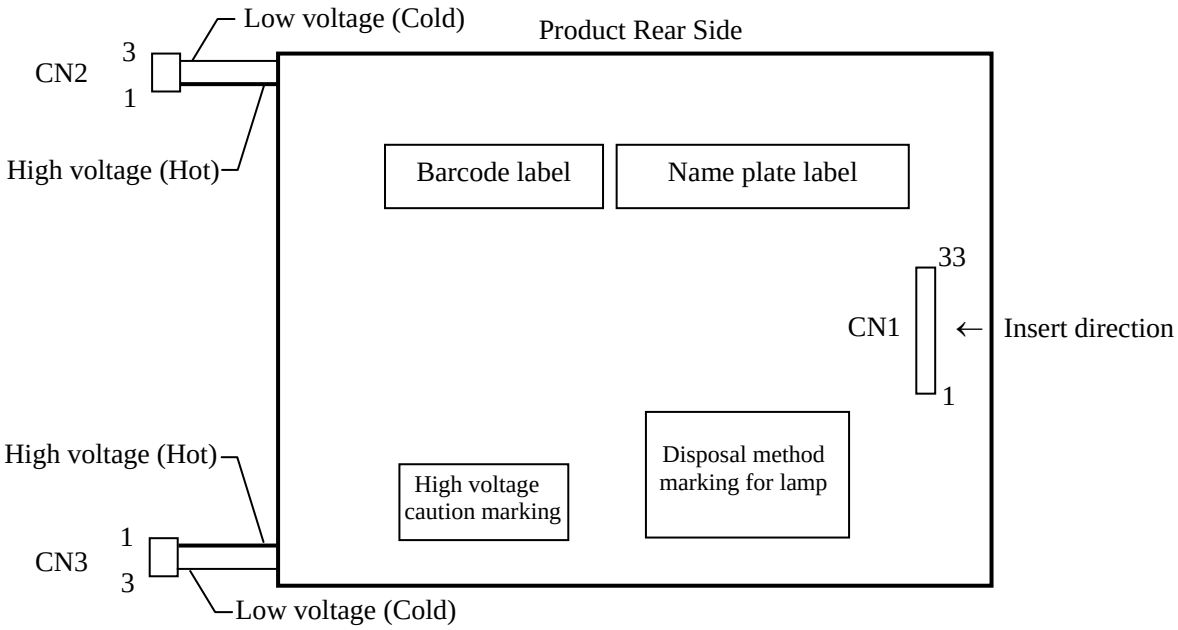
CN2 plug: BHR-03VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM03 (4.0) B-BHS-1-TB (LF) (SN),
SM03 (4.0) B-BHS-1-TB (J.S.T. Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Pink
2	N.C.	-	Keep this pin open.
3	VBLC	Low voltage (Cold)	Cable color: White

CN3 plug: BHR-03VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM03 (4.0) B-BHS-1-TB (LF) (SN),
SM03 (4.0) B-BHS-1-TB (J.S.T. Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Pink
2	N.C.	-	Keep this pin open.
3	VBLC	Low voltage (Cold)	Cable color: White

4.5.3 Positions of plugs and a socket



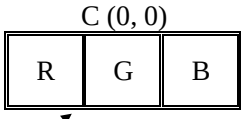
4.6 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 262,144 colors in 64 gray scales. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

4.7 DISPLAY POSITIONS

The following table is the coordinates per pixel (See "**4.8 SCANNING DIRECTIONS**".).



C(0, 0)	C(1, 0)	• • •	C(X, 0)	• • •	C(318, 0)	C(319, 0)
C(0, 1)	C(1, 1)	• • •	C(X, 1)	• • •	C(318, 1)	C(319, 1)
• • •	• • •	• • •	• • •	• • •	• • •	• • •
C(0, Y)	C(1, Y)	• • •	C(X, Y)	• • •	C(318, Y)	C(319, Y)
• • •	• • •	• • •	• • •	• • •	• • •	• • •
C(0,238)	C(1,238)	• • •	C(X,238)	• • •	C(318, 238)	C(319, 238)
C(0,239)	C(1,239)	• • •	C(X,239)	• • •	C(318, 239)	C(319, 239)

4.8 SCANNING DIRECTIONS

4.8.1 QVGA mode

The following figures are seen from a front view. Also the arrow shows the direction of scan.

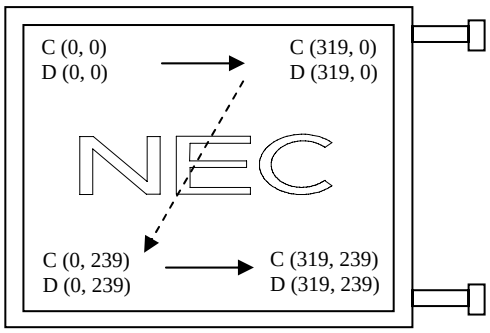


Figure1. DPSH= Low or Open (Normal scan)
DPSV= Low or Open (Normal scan)

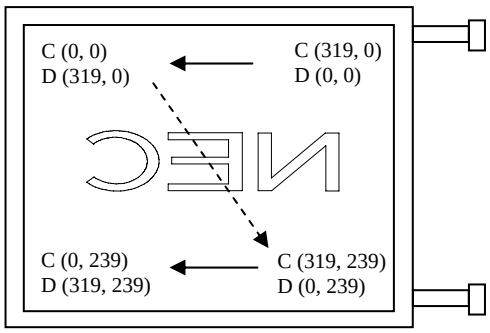


Figure2. DPSH= High (Reverse scan)
DPSV= Low or Open (Normal scan)

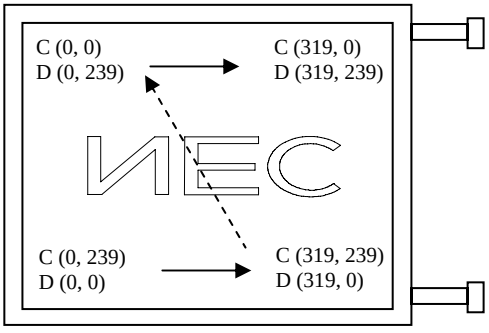


Figure3. DPSH= Low or Open (Normal scan)
DPSV= High (Reverse scan)

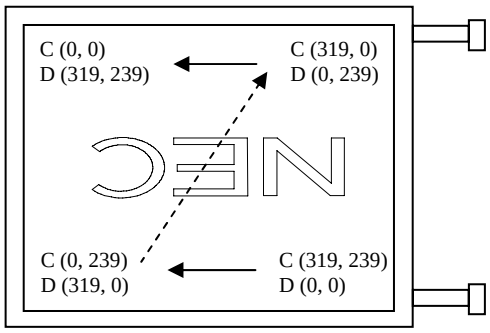


Figure4. DPSH= High (Reverse scan)
DPSV= High (Reverse scan)

Note1: Meaning of C (X, Y) and D (X, Y)
C (X, Y): The coordinates of the display position (See "**4.7 DISPLAY POSITIONS**".)
D (X, Y): The data number of input signal for LCD panel signal processing board

4.8.2 VGA mode

The following figures are seen from a front view. Also the arrow shows the direction of scan. In the VGA mode, only quarter of VGA data signals (640×480) are displayed on the screen.

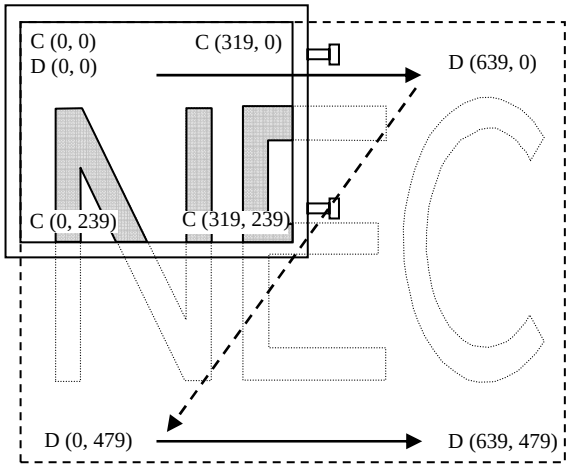


Figure1. DPSH= Low or Open (Normal scan)
DPSV= Low or Open (Normal scan)

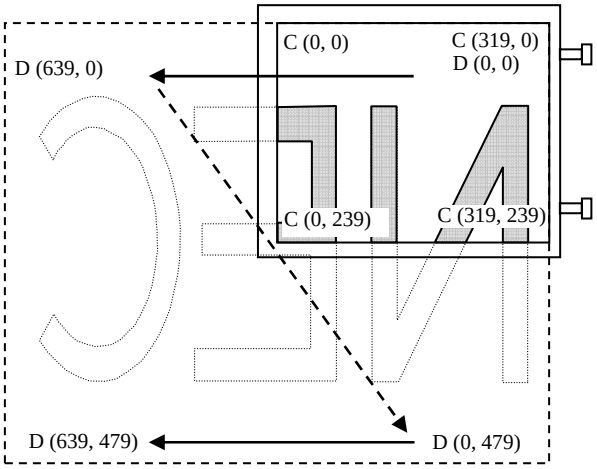


Figure2. DPSH= High (Reverse scan)
DPSV= Low or Open (Normal scan)

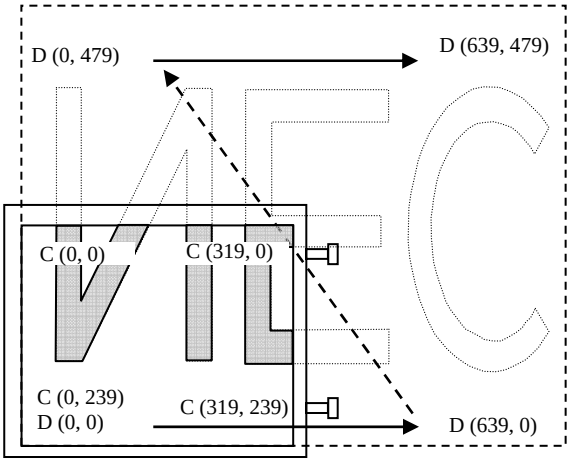


Figure3. DPSH= Low or Open (Normal scan)
DPSV= High (Reverse scan)

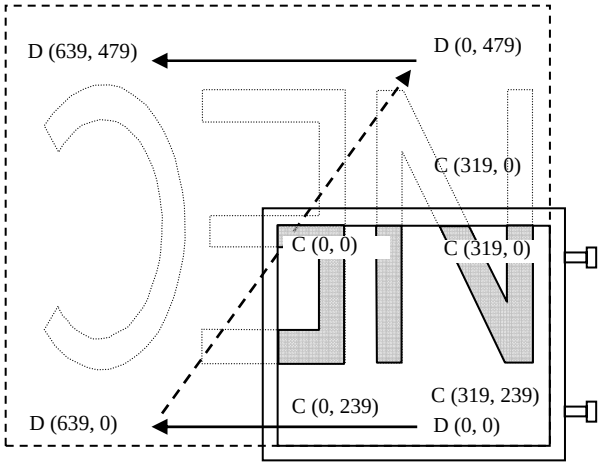


Figure4. DPSH= High (Reverse scan)
DPSV= High (Reverse scan)

Note1: Meaning of C (X, Y) and D (X, Y)
C (X, Y): The coordinates of the display position (See "**4.7 DISPLAY POSITIONS**".)
D (X, Y): The data number of input signal for LCD panel signal processing board

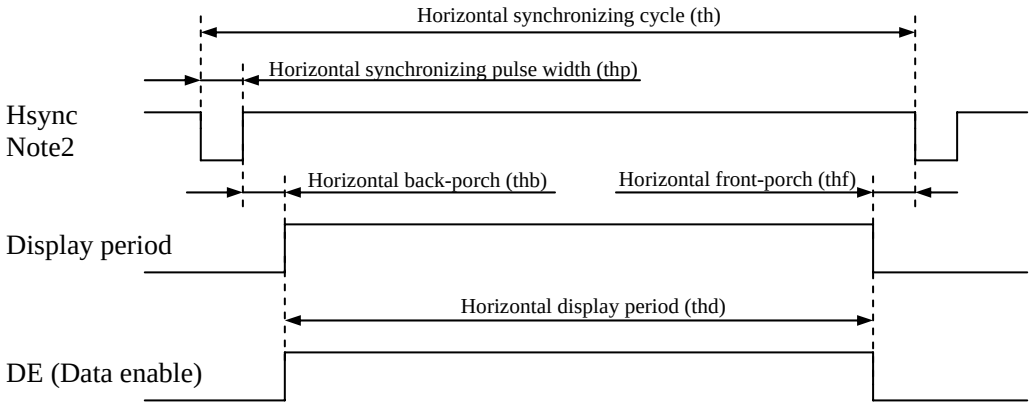
4.9 INPUT SIGNAL TIMINGS

4.9.1 QVGA mode

(1) Outline of input signal timings

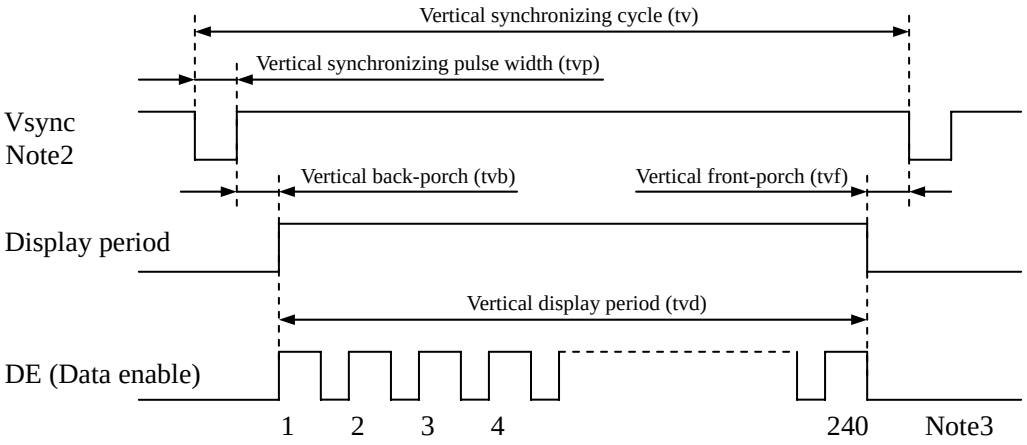
- Horizontal signal

Note1



- Vertical signal

Note1



Note1: This diagram indicates virtual signal for set up to timing.
Note2: Fixed mode cannot be used while working of DE mode.
Note3: See "**4.9.1 (3) Input signal timing chart**" for numeration of pulse.

(2) Timing characteristics

(a) Fixed mode

(Note1)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	5.0	6.4	7.0	MHz	157.5ns (typ.)
	Duty		tcd	0.4	-	0.6	-	-
	Rise time, Fall time		tcrf	-	-	10	ns	
DATA (R0-R5) (G0-G5) (B0-B5)	CLK-DATA	Setup time	tds	5	-	-	ns	-
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Hsync	Cycle		th	57.7	63.5	80.8	µs	15.7kHz (typ.)
				404			CLK	-
	Display period		thd	320			CLK	
	Front-porch		thf	7			CLK	
	Pulse width		thp	3	-	76	CLK	
	Back-porch		thb	1	-	74	CLK	
	Total of pulse width and back-porch		thp + thb	77			CLK	Note2
	CLK-Hsync	Setup time	ths	5	-	-	ns	-
		Hold time	thh	10	-	-	ns	
	Rise time, Fall time		thrf	-	-	10	ns	
Vsync	Cycle		tv	15.1	16.6	21.2	ms	60.1Hz (typ.)
				262			H	-
	Display period		tvd	240			H	
	Front-porch		tvf	1			H	
	Pulse width		tvp	2	-	20	H	
	Back-porch		tvb	1	-	19	H	
	Total of pulse width and back-porch		tvp + tvb	21			H	Note2
	Hsync-Vsync timing		thv	1	-	-	CLK	-
	Vsync-Hsync timing		tvh	10	-	-	ns	
	Rise time, Fall time		tvrf	-	-	10	ns	

Note1: Definition of parameters is as follows.
tc= 1CLK, tcd= tch/tc, th= 1H

Note2: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

(b) DE mode

(Note1, Note2)

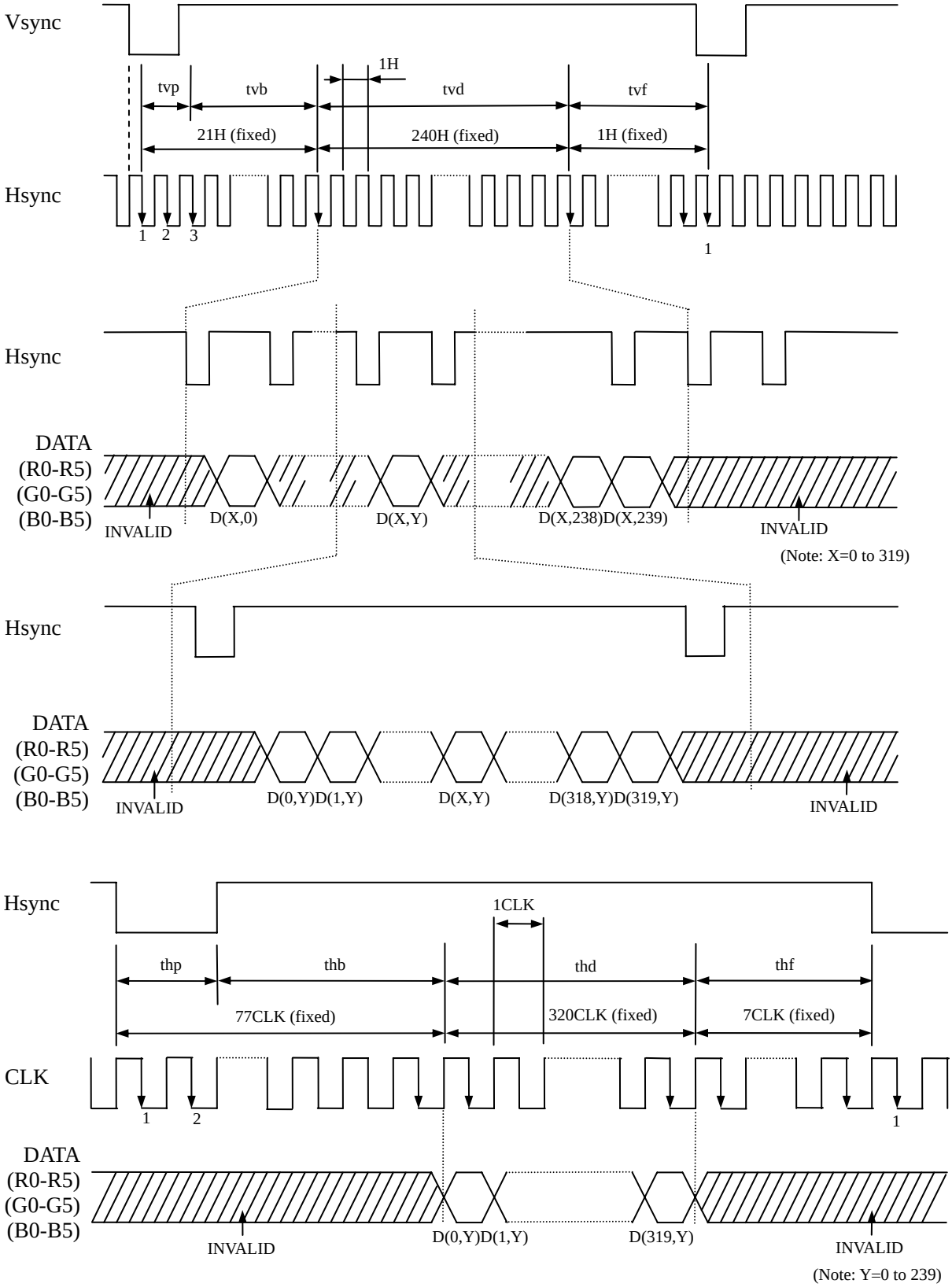
Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	5.0	6.4	7.0	MHz	157.5ns (typ.)
	Duty		tcd	0.4	-	0.6	-	-
	Rise time, Fall time		tcrf	-	-	10	ns	
DATA (R0-R5) (G0-G5) (B0-B5)	CLK-DATA	Setup time	tds	5	-	-	ns	-
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Vsync	Pulse width		tvp	2	-	20	H	-
	Vsync-DE	Setup time	tvds	1	-	-	CLK	
		Hold time	tvdh	1	-	-	CLK	
	Rise time, Fall time		tvrf	-	-	10	ns	
DE	Horizontal	Cycle	th	57.7	63.5	80.8	μs	15.7kHz (typ.)
				331	404	-	CLK	-
		Display period	thd	320			CLK	
	Vertical (One frame)	Cycle	tv	15.1	16.6	21.2	ms	60.1Hz (typ.)
				242	262	-	H	-
		Display period	tvd	240			H	
	CLK-DE	Setup time	tdes	5	-	-	ns	
		Hold time	tdeh	10	-	-	ns	
	Rise time, Fall time		tderf	-	-	10	ns	

Note1: Definition of parameters is as follows.
tc= 1CLK, tcd= tch/tc, th= 1H

Note2: Hsync signal (Pin No.3 of CN1) is not used inside the product at DE mode but do not keep pin open to avoid noise problem.

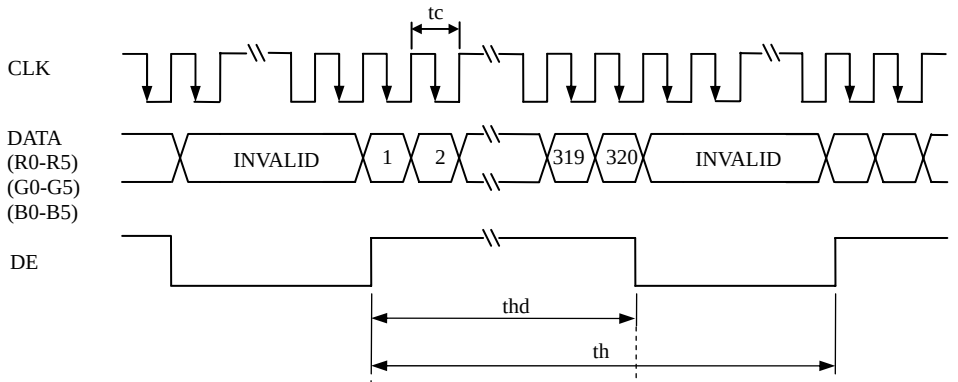
(3) Input signal timing chart

(a) Fixed mode

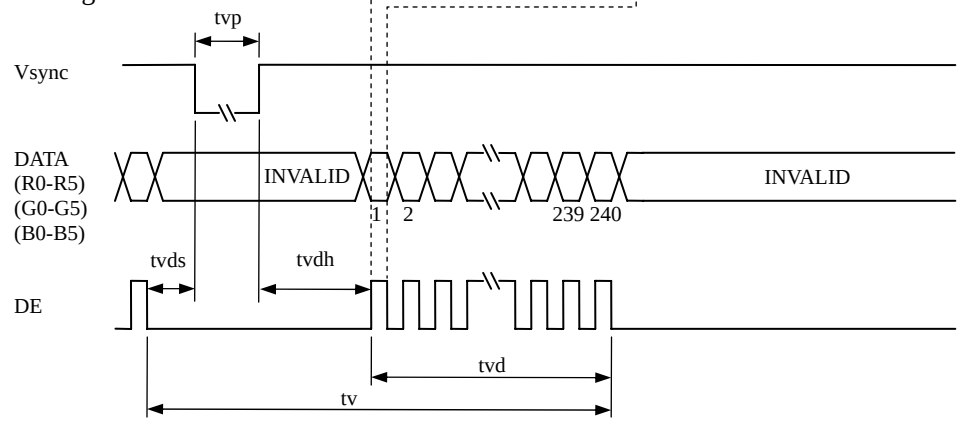


(b) DE mode

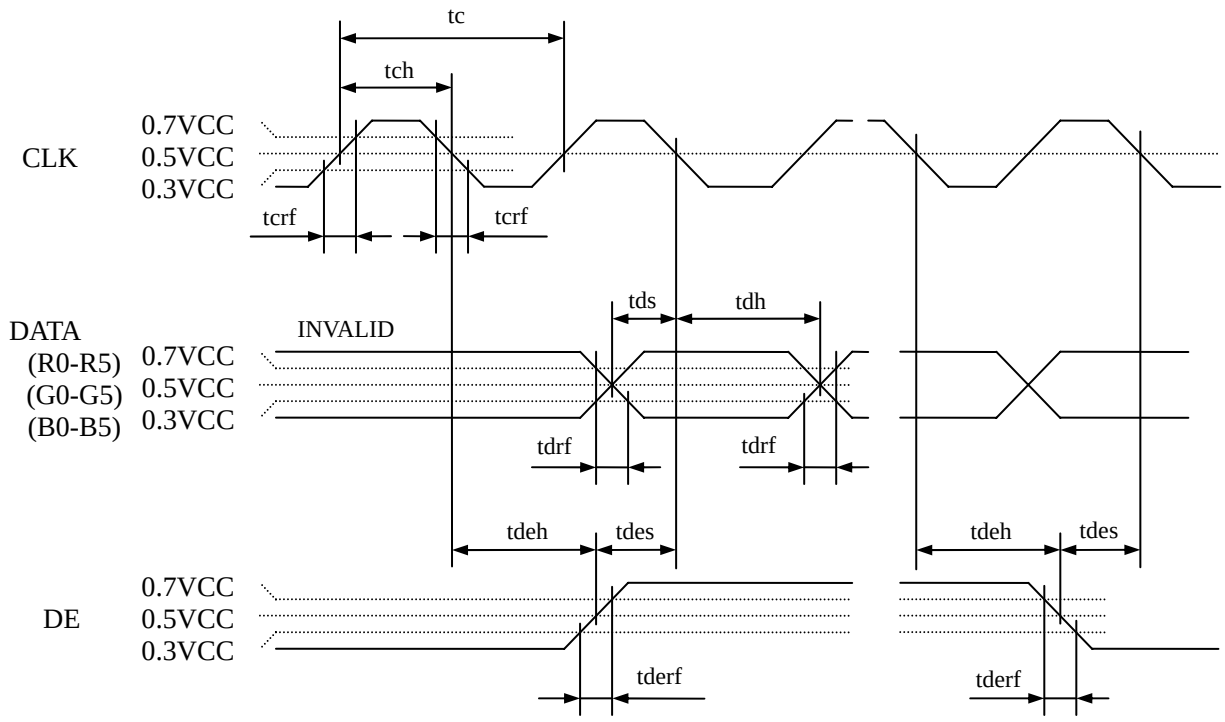
Horizontal timing

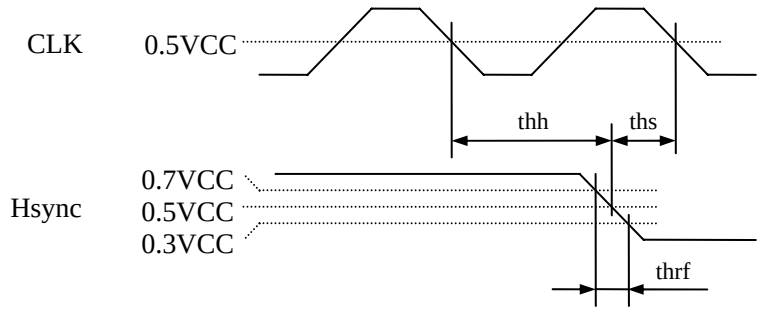


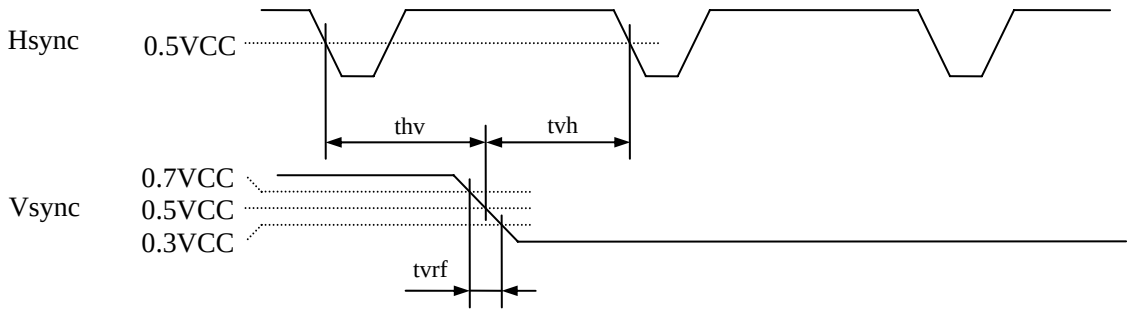
Vertical timing



(c) Common item of Fixed mode and DE mode



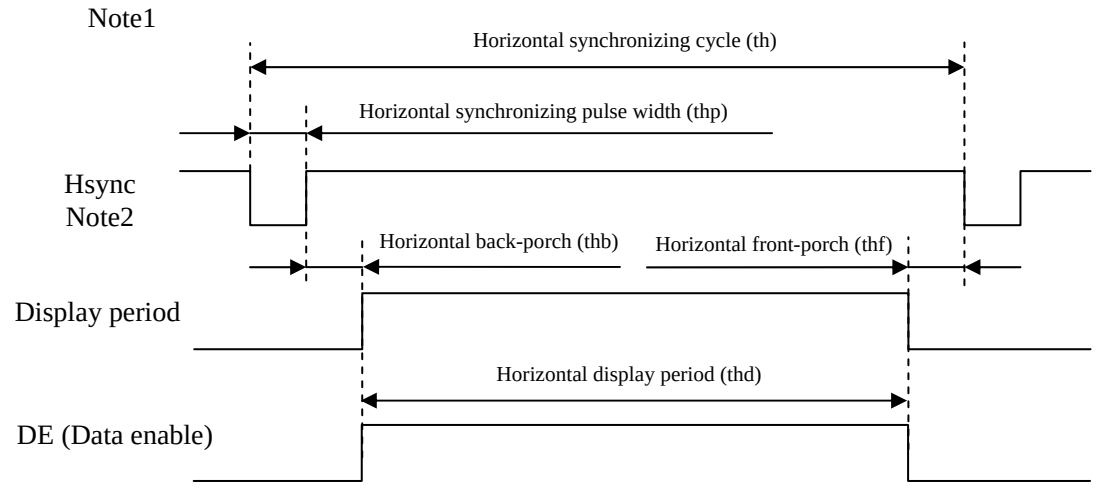




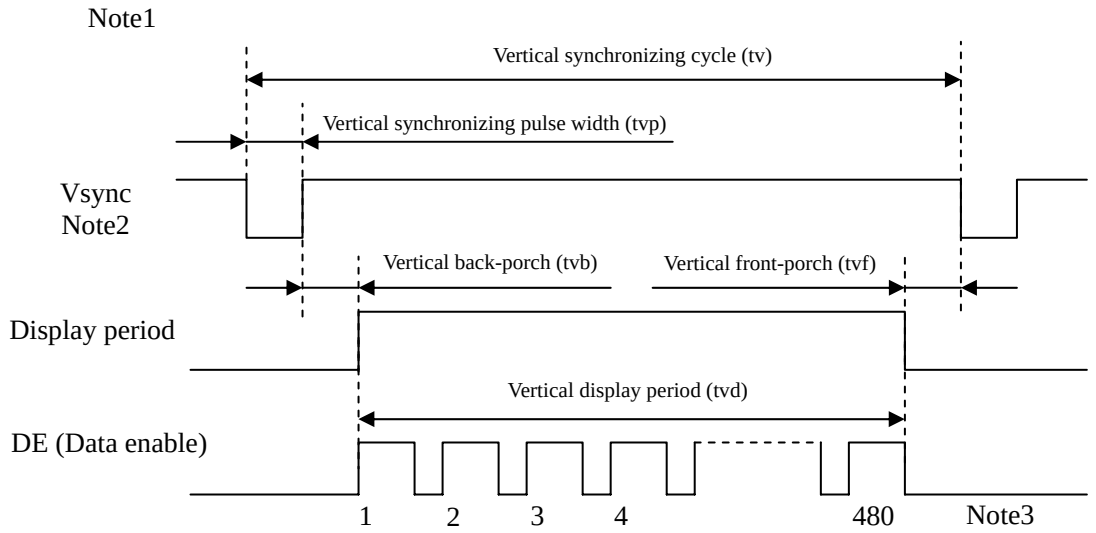
4.9.2 VGA mode

(1) Outline of input signal timings

• Horizontal signal



• Vertical signal



Note1: This diagram indicates virtual signal for set up to timing.
Note2: Fixed mode cannot be used while working of DE mode.
Note3: See "**4.9.2 (3) Input signal timing chart**" for numeration of pulse.

(2) Timing characteristics

(a) Fixed mode

(Note1)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	21.0	25.175	29.0	MHz	39.72ns (typ.)
	Duty		tcd	0.4	0.5	0.6	-	-
	Rise time, Fall time		tcrf	-	-	10	ns	
DATA (R0-R5) (G0-G5) (B0-B5)	CLK-DATA	Setup time	tds	8	-	-	ns	-
		Hold time	tdh	12	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Hsync	Cycle		th	30.0	31.778	33.6	µs	31.468kHz (typ.)
				800			CLK	-
	Display period		thd	640			CLK	
	Front-porch		thf	16			CLK	
	Pulse width		thp	10	96	-	CLK	
	Back-porch		thb	-	48	134	CLK	
	Total of pulse width and back-porch		thp + thb	144			CLK	Note2
	CLK- Hsync	Setup time	ths	8	-	-	ns	-
		Hold time	thh	12	-	-	ns	
	Rise time, Fall time		thrf	-	-	10	ns	
Vsync	Cycle		tv	16.1	16.683	17.2	ms	59.94Hz (typ.)
				525			H	-
	Display period		tvd	480			H	
	Front-porch		tvf	12			H	
	Pulse width		tvp	1	2	-	H	
	Back-porch		tvb	-	31	32	H	
	Total of pulse width and back-porch		tvp + tvb	33			H	Note2
	Hsync-Vsync timing		thv	1	-	-	CLK	-
	Vsync-Hsync timing		tvh	30	-	-	ns	
	Rise time, Fall time		tvrf	-	-	10	ns	

Note1: Definition of parameters is as follows.
tc= 1CLK, tcd= tch/tc, th= 1H

Note2: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

(b) DE mode

(Note1, Note2)

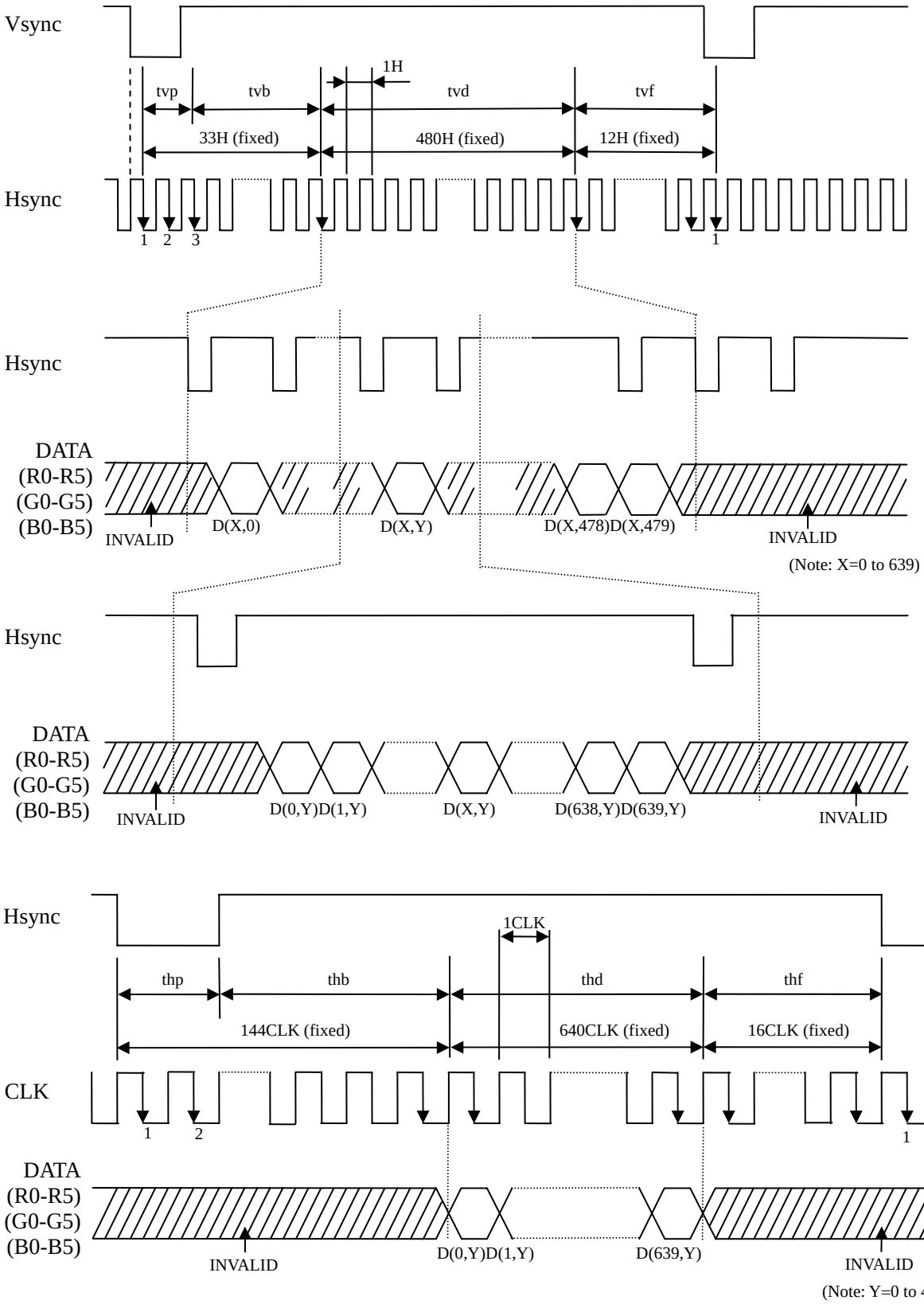
Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	21.0	25.175	29.0	MHz	39.72ns (typ.)
	Duty		tcd	0.4	0.5	0.6	-	-
	Rise time, Fall time		tcrf	-	-	10	ns	
DATA (R0-R5) (G0-G5) (B0-B5)	CLK-DATA	Setup time	tds	8	-	-	ns	-
		Hold time	tdh	12	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Vsync	Pulse width		tvp	1	2	-	H	-
	Vsync-DE timing	Setup time	tvds	1	-	-	CLK	
		Hold time	tvdh	1	-	-	CLK	
	Rise time, Fall time		tvrf	-	-	10	ns	
DE	Horizontal	Cycle	th	30.0	31.778	33.6	µs	31.468kHz (typ.)
				-	800	-	CLK	-
		Display period	thd	640			CLK	
	Vertical (One frame)	Cycle	tv	16.1	16.683	17.2	ms	59.94Hz (typ.)
				-	525	-	H	-
		Display period	tvd	480			H	
	CLK-DE	Setup time	tdes	8	-	-	ns	-
		Hold time	tdeh	12	-	-	ns	
	Rise time, Fall time		tderf	-	-	10	ns	

Note1: Definition of parameters is as follows.
tc= 1CLK, tcd= tch/tc, th= 1H

Note2: Hsync signal (Pin No.3 of CN1) is not used inside the product at DE mode.
Do not keep pin open to avoid noise problem.

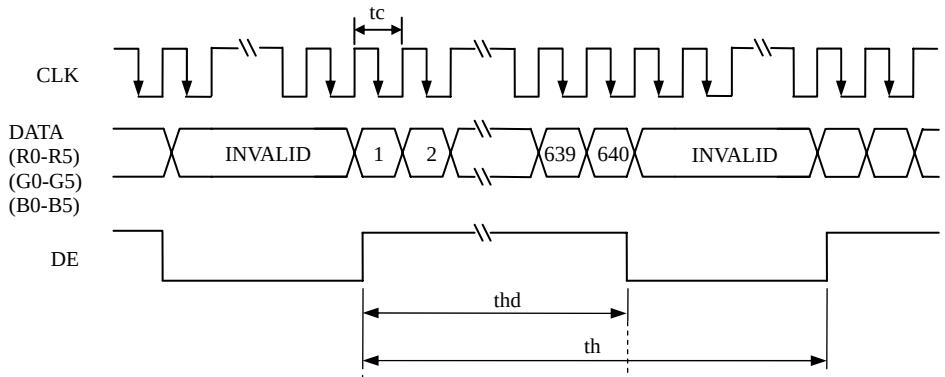
(3) Input signal timing chart

(a) Fixed mode

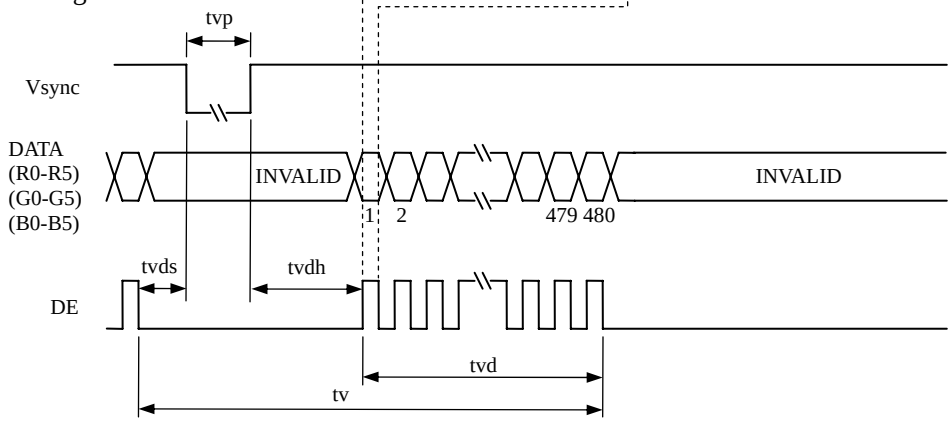


(b) DE mode

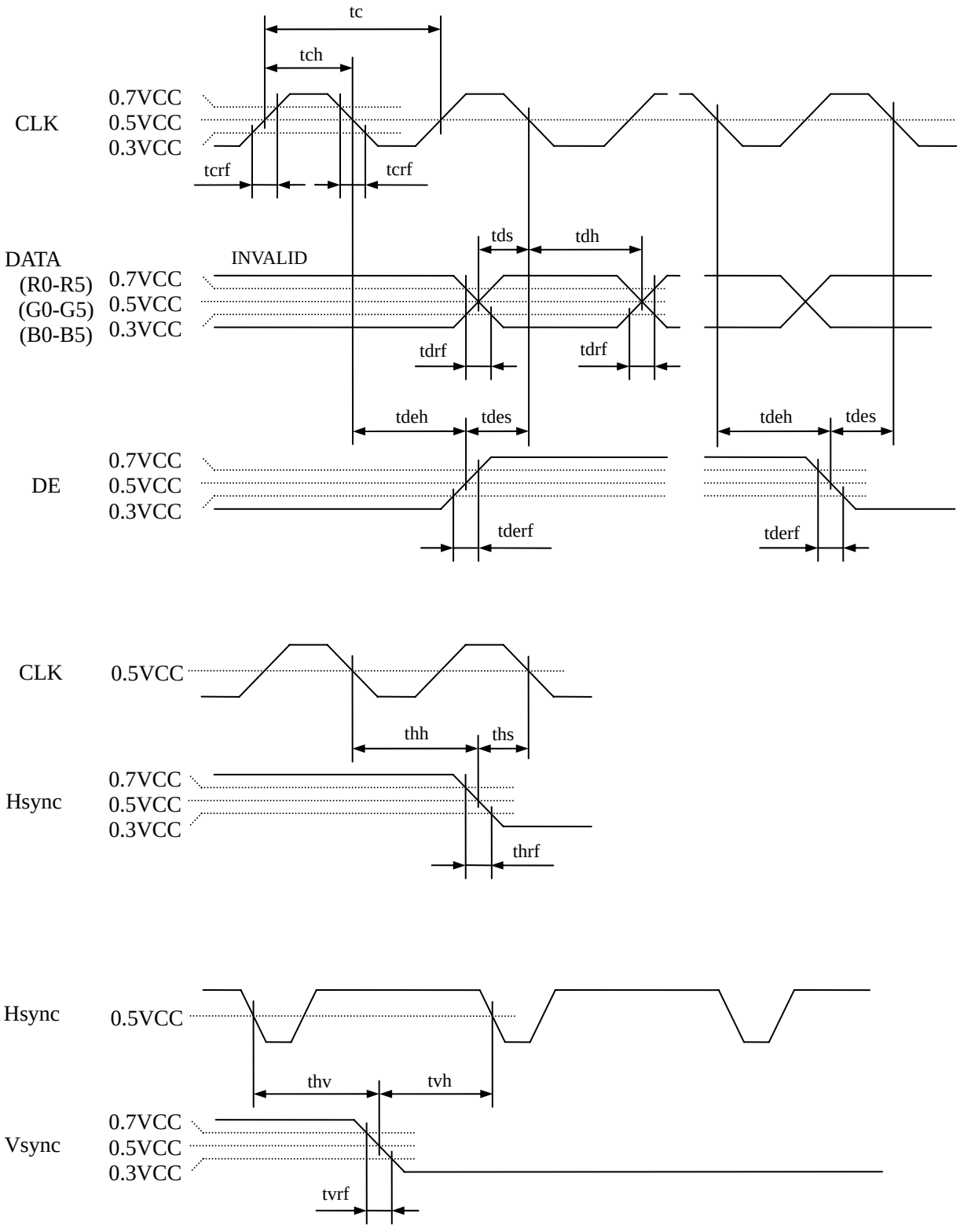
Horizontal timing



Vertical timing



(c) Common item of Fixed mode and DE mode



4.10 OPTICS

4.10.1 Optical characteristics

Optical characteristics are only applied to the QVGA mode. The VGA mode is exempted from the assurance.

(Note1, Note2)

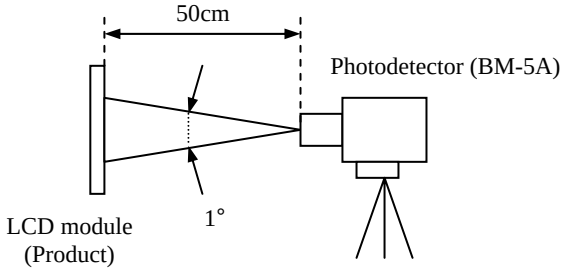
Parameter		Condition	Symbol	min.	typ.	max.	Unit	Remarks
Luminance		White at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	L	550	750	-	cd/m^2	-
Contrast ratio		White/Black at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	CR	320	500	-	-	Note3
Luminance uniformity		White θR= 0°, θL= 0°, θU= 0°, θD= 0°	LU	-	1.25	1.35	-	Note4
Chromaticity	White	**x** coordinate	Wx	0.270	0.300	0.330	-	Note5
		y coordinate	Wy	0.310	0.340	0.370	-	
	Red	**x** coordinate	Rx	-	0.615	-	-	
		y coordinate	Ry	-	0.350	-	-	
	Green	**x** coordinate	Gx	-	0.320	-	-	
		y coordinate	Gy	-	0.575	-	-	
	Blue	**x** coordinate	Bx	-	0.150	-	-	
		y coordinate	By	-	0.130	-	-	
Color gamut		θR= 0°, θL= 0°, θU= 0°, θD= 0° at center, against NTSC color space	C	40	50	-	%	
Response time		White to Black	Ton	-	5	15	ms	Note6 Note7
		Black to White	Toff	-	25	50	ms	
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	45	55	-	°	Note8
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	45	55	-	°	
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	40	50	-	°	
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	30	40	-	°	

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta= 25°C, VCC= 3.3V, IBL= 5.0mArms/lamp, QVGA, Horizontal cycle= 1/15.7kHz, Vertical cycle= 1/60.1Hz, DPSH= Open, DPSV= Open, Q/V= Low or Open: QVGA mode

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "**4.10.2 Definition of contrast ratio**".

Note4: See "**4.10.3 Definition of luminance uniformity**".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF= 33°C

Note7: See "**4.10.4 Definition of response times**".

Note8: See "**4.10.5 Definition of viewing angles**".

4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

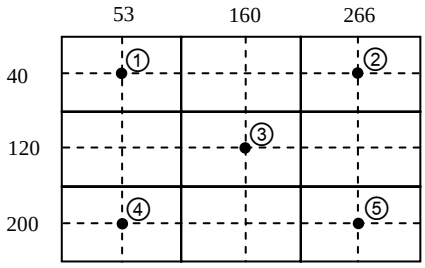
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

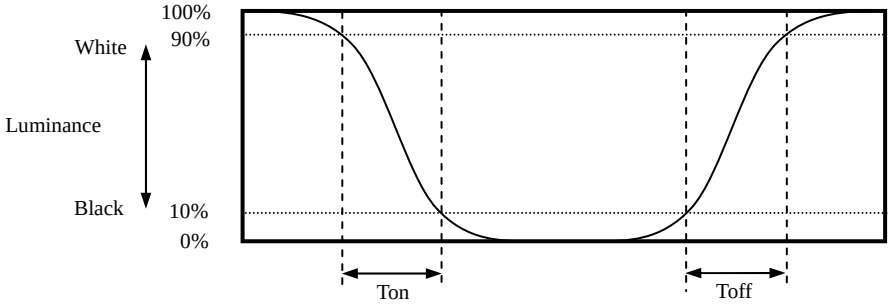
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

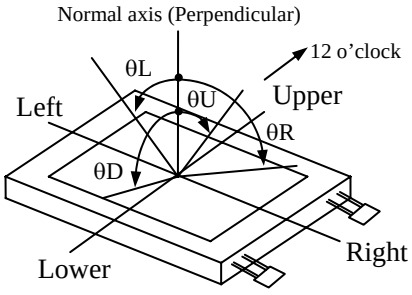


4.10.4 Definition of response times

Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 90% down to 10%. Also Toff is the time it takes the luminance change from 10% up to 90% (See the following diagram.).



4.10.5 Definition of viewing angles



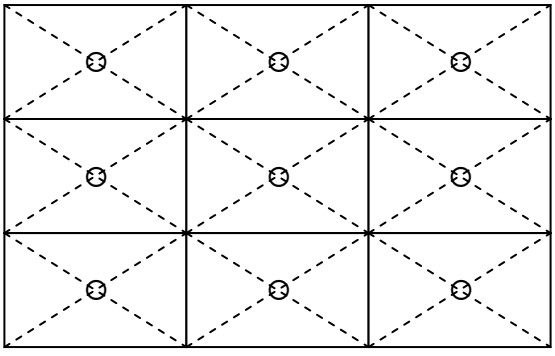
5. RELIABILITY TESTS

Reliability tests are only applied to the QVGA mode. The VGA mode is exempted from the assurance.

Test item	Condition	Judgment
High temperature and humidity (Operation)	① 55 ± 2°C, RH = 85%, 240hours ② Display data is black.	No display malfunctions Note1
High temperature (Operation)	① 70 ± 3°C, 240hours ② Display data is black.	
Heat cycle (Operation)	① -10 ± 3°C…1hour 70 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is black.	
Thermal shock (Non operation)	① -30 ± 3°C…30minutes 80 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
ESD (Operation)	① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	
Dust (Operation)	① Sample dust: No. 15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Vibration (Non operation)	① 5 to 200Hz, 29.4m/s^2 ② 10 minutes/cycle ③ X, Y direction…2hours ④ Z direction…4hours	No display malfunctions No physical damages Note1
Mechanical shock (Non operation)	① 980m/ s^2, 11ms ② ±X, ±Y, ±Z direction ③ 3 times each directions	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points.

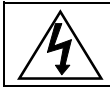


6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.



This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

- **Do not touch the working backlight. There is a danger of an electric shock.**

- **Do not touch the working backlight. There is a danger of burn injury.**
- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 980m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6 N (ϕ16mm jig))**

6.3 ATTENTIONS

6.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
③ When the product is put on the table temporarily, display surface must be placed downward.
④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
⑤ The torque for product mounting screws must never exceed 0.294N·m. Higher torque might result in distortion of the bezel.
⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
⑧ Do not push nor pull the interface connectors while the product is working.

⑨ Do not bend or unbend the lamp cable at the near part of the lamp holding rubber, to avoid the damage for high voltage side of the lamp.
⑩ Properly connect the plug (backlight side) to adaptable socket (inverter side) without incomplete connection. After connecting, be careful not to hook the lamp cables because incomplete connection may occur by hooking the lamp cables. This incomplete connection may cause abnormal operation of high voltage circuit. ☆
⑪ If the lamp cable is attached on the metal part of the product directly, high frequency leak current to the metal part may occur, then the brightness may decrease or the lamp may not be turned on.
⑫ When not connecting shield plate of the LCD module to the customer's equipment ground, inverter noise may create video noise on the LCD screen.
⑬ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
⑭ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal for the worst, please wash it out with soap. ☆

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.

6.3.3 Characteristics

The following items are neither defects nor failures.

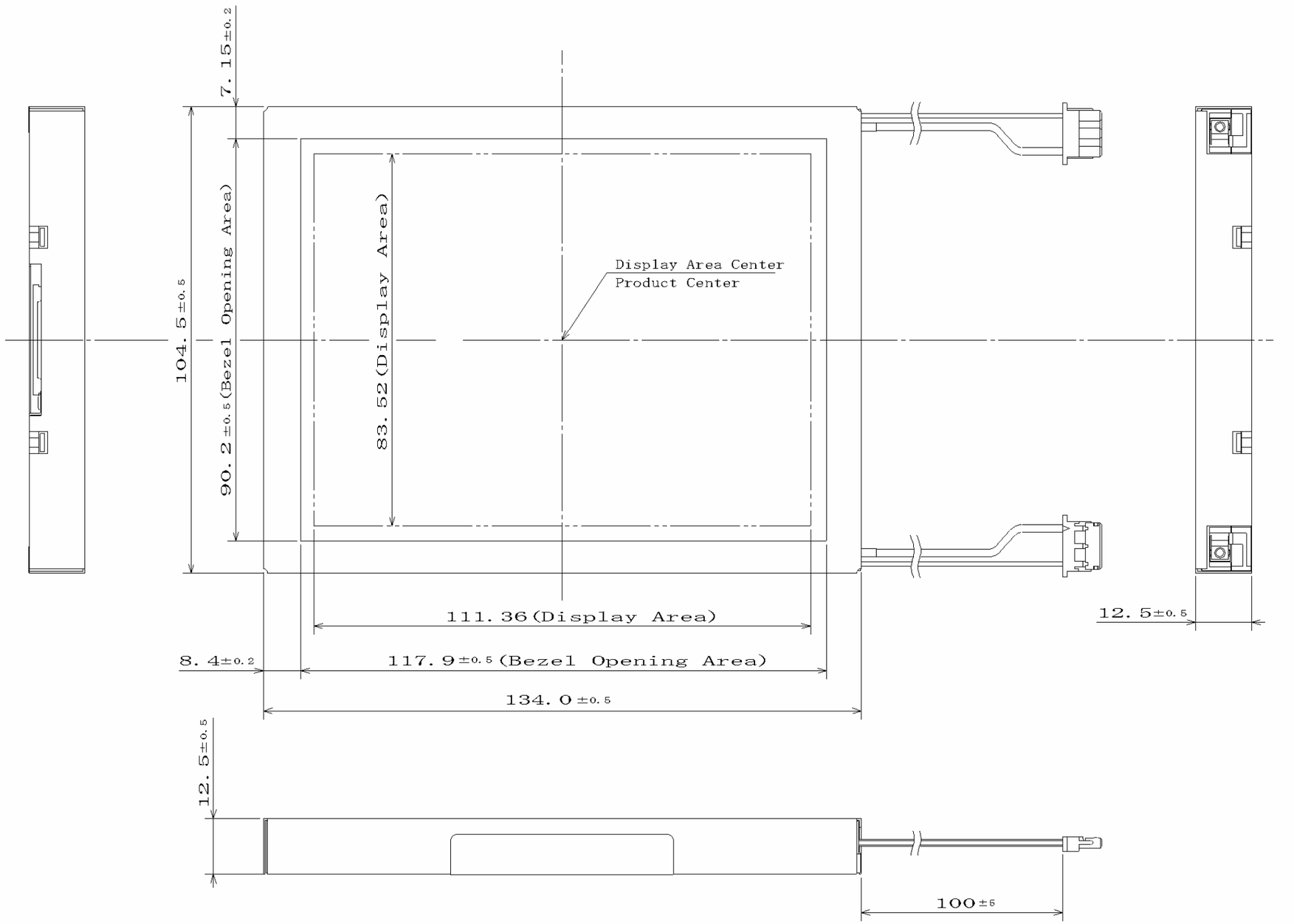
① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed depending on input signal timings.
⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.
⑧ The color of the polarizer surface may differ between products because of antireflection treatment.
⑨ After the product is stored under condition of low temperature or dark place for a long time, the cold cathode fluorescent lamp may not be turned on under the same condition because of the general characteristic of cold cathode fluorescent lamp. In addition, when Luminance control ratio is low in pulse width modulation method inverter, the lamp may not be turned on. In this case, power should be supplied again. ☆

6.3.4 Other

① All GND and VCC terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ See "REPLACEMENT MANUAL FOR LAMP HOLDER SET", when replacing backlight lamps.
④ Pay attention not to insert foreign materials inside of the product, when using tapping screws.
⑤ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.

7. OUTLINE DRAWINGS

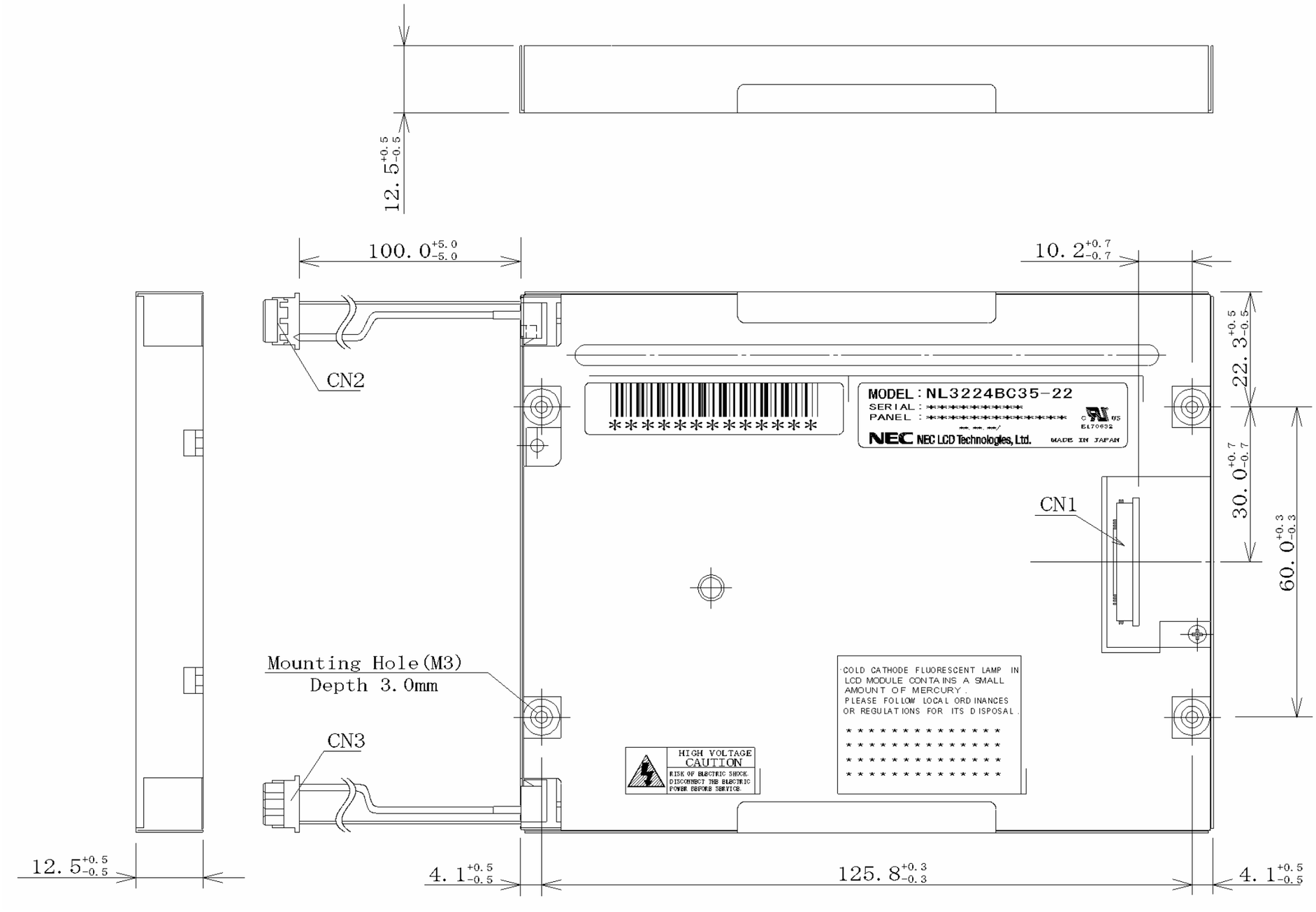
7.1 FRONT VIEW



Unit: mm

Note1: The torque for product mounting screws must never exceed 0.294N·m.

7.2 REAR VIEW



Unit: mm

Note1: The torque for product mounting screws must never exceed 0.294N·m.