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HITACHI

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FOR MESSRS : _____ DATE : May.13,2008

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

TX14D12VM1CBA

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*When product will be discontinued, customer will be informed by HITACHI with twelve months prior to discontinuation.

ACCEPTED BY; _____ PROPOSED BY: Dan Cheng

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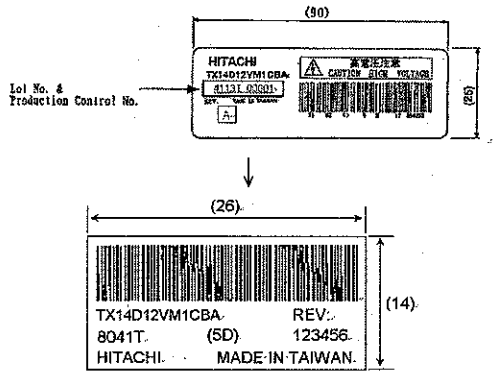
May.13,'08	7B64PS 2708-TX14D12VM1CBA-5 PAGE 8-6/6	8.5 INTERNAL PIN CONNECTION Changed : CN1 JAE : FA5B040HF1R3000(Sn plating) → FA5B040HP1R3000(Au plating)
	7B64PS 2709-TX14D12VM1CBA-5 PAGE 9-1/1	9. DIMENSIONAL OUTLINE The lot label size and position is changed.
	7B64PS 2712-TX14D12VM1CBA-5 PAGE 12-1/1	12.1 LOT MARK Changed : 5 digits for production number ↓ 6 digits for production number 12.3 LOCATION OF LOT MARK Changed :  12.4 REVISION(Rev.) CONTROL Added : Rev. C CN1 JAE : FA5B040HP1R3000

3.GENERAL DATA

The specifications are applied to the following TFT-LCD Module with Back-light unit.
Note : Inverter device for Back-light is not built in this Module.

(1)	Part Name	TX14D12VM1CBA
(2)	Module Dimensions	131.0(W)mm x 102.2(H)mm x 10.9(D)mm typ.
(3)	LCD Active Area	115.2(W)mm x 86.4(H)mm
(4)	Dot Pitch	0.12(W)mm x 3(R,G,B)(W) x 0.36(H)mm
(5)	Resolution	320x3(R,G,B))(W)x240(H) dots
(6)	Color Pixel Arrangement	R,G,B Vertical stripe
(7)	LCD Type	Transmissive Color TFT LCD (Normally White)
(8)	Display Type	Active Matrix
(9)	Number of Colors	262k Colors (R,G,B 6bit digital each)
(10)	Backlight	Cold Cathode Fluorescent Tube (L shaped CFL) x 1
(11)	Weight	(160)g (typ.)
(12)	Interface	40pin (C-MOS)
(13)	Power Supply Voltage	3.3V only (Include Timing Controller and Power Unit)
(14)	Viewing Direction	6 O'clock (The direction it's hard to be discolored)

4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD VSS=0V

ITEM	SYMBOL	MIN.	MAX.	UNIT	COMMENT
Power Supply for Logic	VDD	-0.3	4.0	V	
Input Voltage	VI	-0.3	VDD+0.3		(Note 1)
Input Current	Ii	0	1	A	
Static Electricity	VESD0	-	±100	V	(Note 2,3)
	VESD1	-	±8	kV	(Note 2,4)

Note 1 : DTMG,DCLK,RD0~RD5,GD0~GD5,BD0~BD5.
Note 2 : 200pF-250Ω 25℃ - 70%RH
Note 3 : Interface Pin Connector.
Note 4 : The surface of metal bezel and LCD panel .

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

I T E M	OPERATING		STORAGE		COMMENT
	MIN.	MAX.	MIN.	MAX.	
Temperature	(-20)	(70)	(-30)	(80)	(Note 2,3,6,7,8,10,12)
Humidity	(Note 1)		(Note 1)		Without condensation
Vibration	-	4.9m/s^2 (0.5G)	-	19.6m/s^2 (2G) (Note 5)	(Note 4)
Shock	-	29.4m/s^2 (3G)	-	490m/s^2 (50G) (Note 5)	XYZ directions (Note 9)
Corrosive Gas	Not Acceptable		Not Acceptable		
CFL Life Time	50,000 h (Average) (Note 11)		-		At 25℃ , IL=5.0mA max.

Note 1 : Ta≦40℃ :85%RH max.
Ta＞40℃ :Absolute humidity must be lower than the humidity of 85%RH at 40℃.
Note 2 : For storage condition Ta at -30℃ ＜ 48h , at 80℃ ＜ 100h.
For operating condition Ta at -20℃ ＜ 100h
Note 3 : Background color changes slightly depending on ambient temperature.
This phenomenon is reversible.
Note 4 : 5Hz~100Hz(Except resonance frequency)
Note 5 : This LCM will resume normal operation after finishing the test.
Note 6 : The response time will be slower at low temperature.
Note 7 : Only operation is guarantied at operating temperature. Contrast, response time, another display quality are evaluated at +25℃.
Note 8 : When LCM is operated over 60℃ ambient temperature , the ICFL of LCM should be adjusted to 3mA max.
Note 9 : Pulse Width : 10ms
Note 10 : This is panel surface temperature , not ambient temperature.
Note 11 : When brightness reached 50% of initial brightness.
Note 12 : When LCM be operated less than 0℃ , the life time of CFL will be reduced .
The rise time of CFL ON will be longer when the ambient temperature below 0℃ and confirming the characteristics of inverter is necessary .

4.3 BACK-LIGHT UNIT

Item	Symbol	Min.	Max.	UNIT	COMMENT
Lamp Current	IL	-	7.0	m Arms	(Note 1)
Lamp Voltage	VL	-	3000	Vrms	(Note 2)

Note 1 : Please put your meter at GND cable to measurement.
Note 2 : Apply to the connector of the back light unit.

5. ELECTRICAL CHARACTERISTICS

5.1 ELECTRICAL CHARACTERISTICS OF LCD

Ta=25℃,VSS=0V

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	VDD	-	3.0	3.3	3.6	V
Input Voltage for Logic (Note 1)	VI	"H" level	2.0	-	VDD	V
		"L" level	VSS	-	0.8	
Power Supply Current (Note 2)	IDD	VDD-VSS=3.3V	-	(65)	-	mA
Vsync Frequency	fV	-	52	60	68	Hz
Hsync Frequency	fH for VGA display mode	-	25.3	29.5	36.1	kHz
	fH for QVGA display mode		13.1	15.2	17.7	
DCLK Frequency	fCLK for VGA display mode	-	17.2	20.9	26.7	MHz
	fCLK for QVGA display mode		4.85	5.85	7.0	

Note 1 : DTMG,DCLK, RD0~RD5,GD0~GD5,BD0~BD5.
Note 2 : f V=60Hz,Ta=25℃, Pattern used as display pattern : All Black.
Note 3 : Need to make sure of flickering and rippling of display when setting the frame frequency in your set.

5.2 ELECTRICAL CHARACTERISTICS OF BACKLIGHT

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Lamp Voltage	VL	-	(760)	-	Vrms	Ta=25℃
Frequency	fL	-	(55)	-	kHz	
Lamp Current (1Lamp)(Note 6,7)	IL	(2.0)	(5.0)	(6.0)	mA	Ta=25℃
Starting Discharge Voltage	VS (Note 2)	(1300)	-	-	Vrms	Ta=5℃

Note 1 : Please design your lamp driving circuit (inverter) according to the above specifications, and inform HITACHI about it.
Note 2 : Starting discharge voltage is increased when LCM is operating under low temperature.
Please check the characteristics of your inverter before applying to your set.
Note 3 : Average life time of CFL will be decreased when LCM is operating under low temperature.
Note 4 : Under lower driving frequency of an inverter, a certain Backlight system (CFL & CFL reflection sheet) may generate a sound noise. Before designing the inverter, please consider the driving frequency and noise.
Note 5 : When IL is over 6.0mA, it may cause uneven contrast near CFL location, due to heat dispersion from CFL.
Note 6 : We recommend to equip protection circuit (To stop output) which works under abnormal operation to the inverter for CFL
Note 7 : Measurement of IL is provided for GND side of CFL.

6. OPTICAL CHARACTERISTICS

6.1 OPTICAL CHARACTERISTICS OF LCD

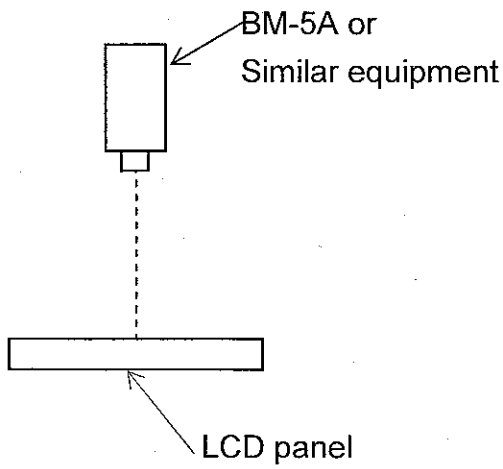
Ta=25℃ (Backlight on)

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Viewing Area		θ x	ϕ=0°,K≧10.0	-	65	-	deg	1~5
		θ x'	ϕ=180°,K≧10.0	-	65	-	deg	1~5
		θ y	ϕ=90°,K≧10.0	-	70	-	deg	1~5
		θ y'	ϕ=270°,K≧10.0	-	50	-	deg	1~5
Contrast Ratio		K	ϕ=0°, θ=0°	120	350	-	-	5
Response Time (rise+fall)		tr+tf	ϕ=0°, θ=0°	-	(45)	-	ms	6
Color Tone (Primary Color)	Red	x	ϕ=0°, θ=0°	0.56	0.61	0.66	-	
		y		0.28	0.33	0.38	-	
	Green	x		0.25	0.30	0.35	-	
		y		0.52	0.57	0.62	-	
	Blue	x		0.09	0.14	0.19	-	
		y		0.03	0.08	0.13	-	
	White	x		0.24	0.29	0.34	-	
		y		0.24	0.29	0.34	-	

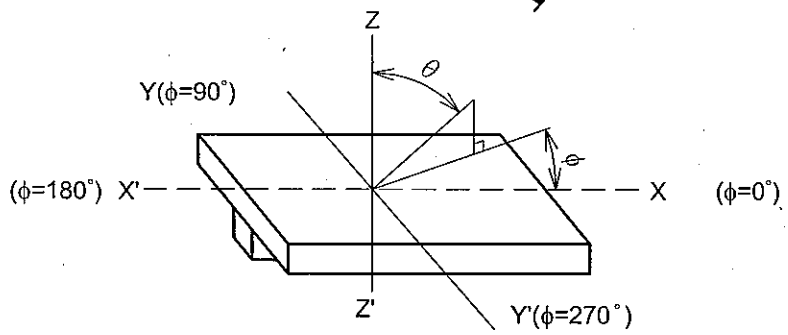
Note 1 : Driving Condition
Display Pattern : White Raster
ICFL Current : (5.0)mA

(Measurement condition : HITACHI standard)
(Note 3~6) : See next page.

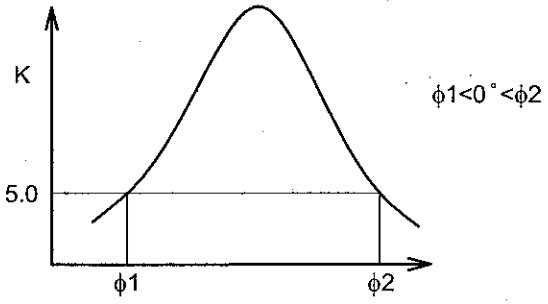
Note 2 : Measurement Condition
(Transmitance)

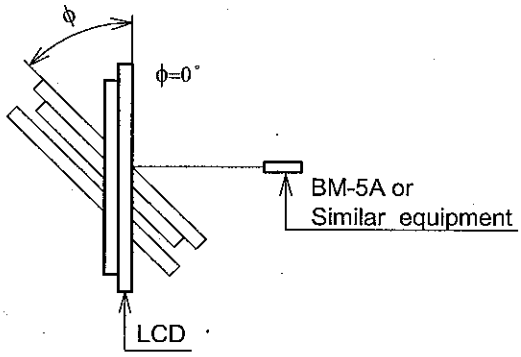


Note 3 : Definition of θ and ϕ
(Normal)
Viewing direction



Note 4 : Definition of Viewing angle $\phi 1$ and $\phi 2$



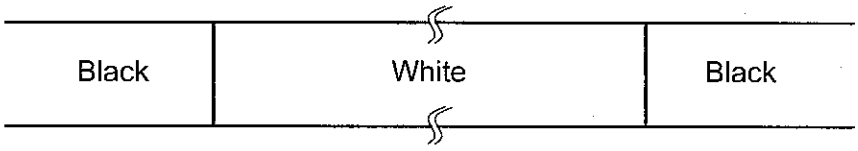


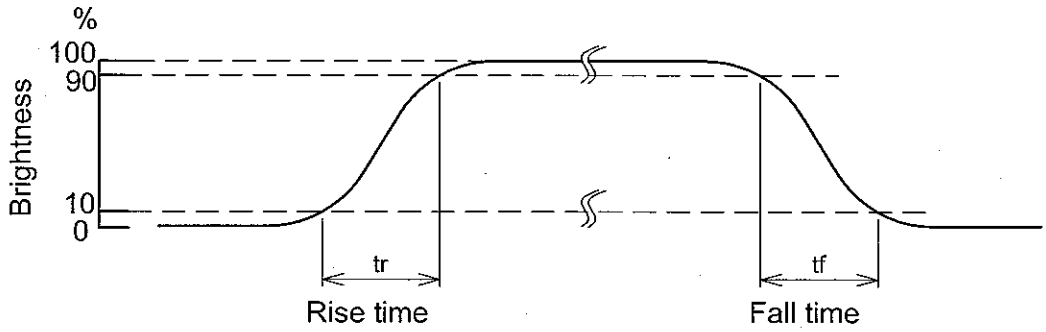
Contrast ratio "K" vs Viewing angle "ϕ"

Note 5 : Definition of contrast "K"

$$K=\frac{\text{White Brightness}}{\text{Black Brightness}}$$

Note 6 : Definition optical response time





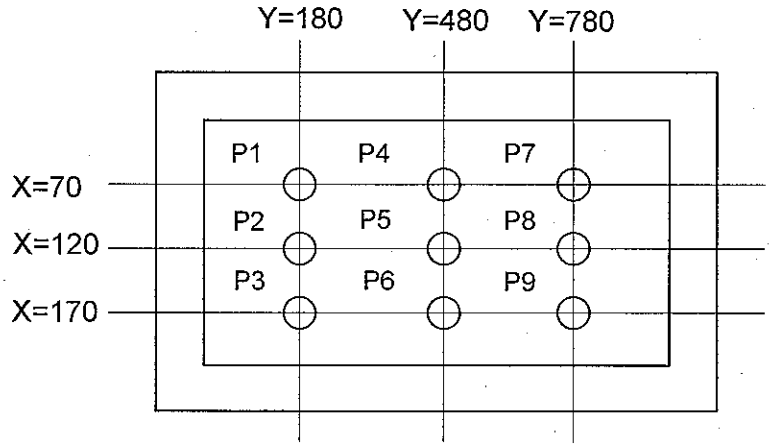
6.2 OPTICAL CHARACTERISTICS OF BACKLIGHT

ITEM	MIN.	TYP.	MAX.	UNIT	NOTE
Brightness	200	350	-	cd/m^2	IL=(5.0)mA (Note 1)
Rise Time	-	3	-	Minute	IL=(5.0)mA Brightness 80%
Brightness Uniformity	-	-	±25	%	Under mentioned (Note 1,3)

(Measurement condition : HITACHI standard)

CFL : 0h operation, Ta=25℃
Display data should be set to all "ON".

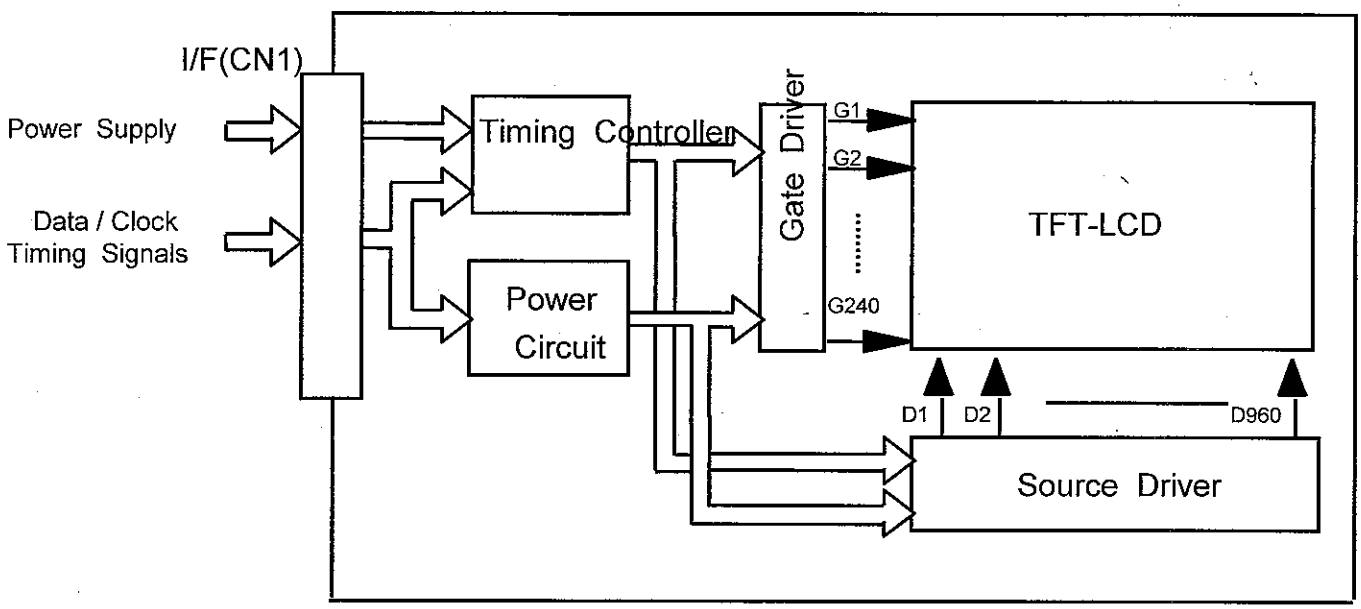
Note 1 : Measurement after 10 minutes from CFL operating.
Active area center.
Note 2 : Brightness control : 100%.
Note 3 : Measurement of the following 9 places on the display.

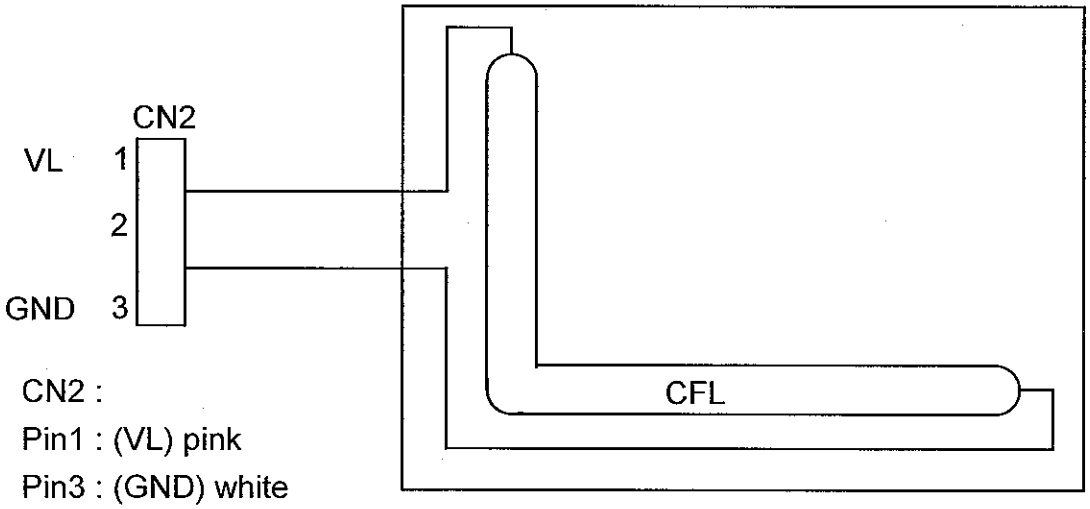


Note 4 : Definition of the brightness tolerance.

$$\left(\frac{\text{Max. brightness or Min. brightness - Average brightness}}{\text{Average brightness}}\right)\times 100$$

7.BLOCK DIAGRAM





CN2 :
Pin1 : (VL) pink
Pin3 : (GND) white

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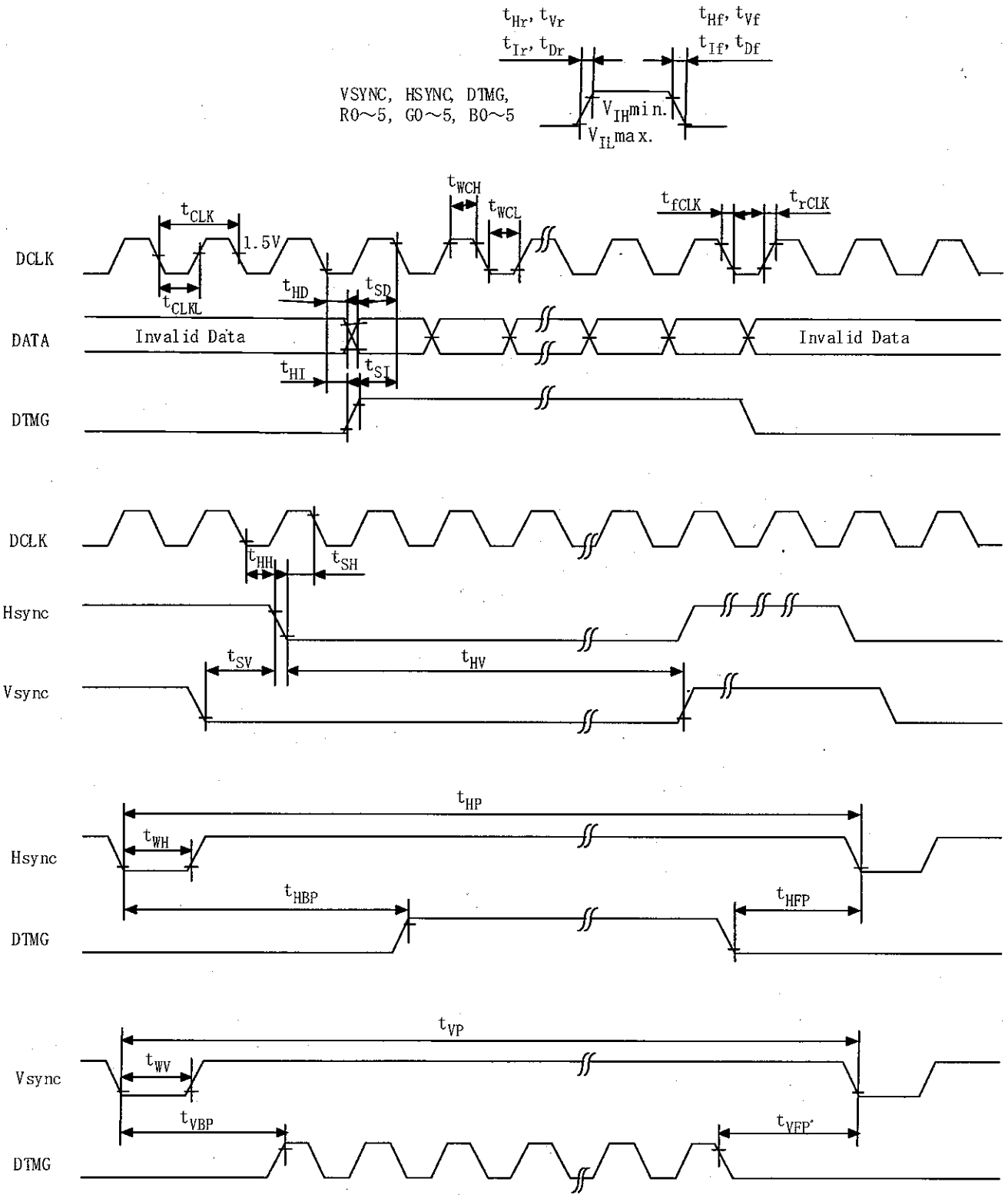
8.INTERFACE TIMING

8.1 Timing Chart

(Data is latched negative edge trigger of DCLK)



Note 1 : DTMG is definition of the above timing for Hsync and Vsync.

Note 2 : No matter when Hsync and Vsync is inputted ,this LCM can be drove only DTMG Signal. DTMG should be set to low level when it is not input valid data.

8.2.1 INTERFACE TIMING FOR QVGA DISPLAY MODE

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
DCLK	Cycle time	t_{CLK}	(60)	(171)	(206)	ns	
	Low level Width	t_{WCL}	12	-	-		
	High level Width	t_{WCH}	12	-	-		
	Rise time	t_{rCLK}	-	-	(20)		
	Fall time	t_{fCLK}	-	-	(20)		
	Duty	D	0.45	0.5	0.55	-	D= t_{CLKL}/ t_{CLK}
Hsync	Set up time	t_{SH}	5	-	-	ns	for DCLK
	Hold time	t_{HH}	10	-	-		
	Cycle	t_{HP}	358	(385)	453	t_{CLK}	
	Valid width	t_{WH}	4	(5)	-		
	Rise/Fall time	t_{Hr},t_{Hf}	-	-	30	ns	
Vsync	Set up	t_{SV}	0	-	-	t_{CLK}	for Hsync
	Hold	t_{HV}	2	-	-		
	Cycle	t_{VP}	247	(253)	535	t_{HP}	
	Valid width	t_{WV}	2	(2)	-		
	Rise/Fall time	t_{Vr},t_{Vf}	-	-	50	ns	
DTMG	Set up time	t_{SI}	5	-	-	ns	for DCLK
	Hold time	t_{HI}	10	-	-		
	Rise/Fall time	t_{Ir},t_{If}	-	-	30	ns	
	Horizontal back porch	t_{HBP}	24	(35)	99	t_{CLK}	
	Horizontal front porch	t_{HFP}	8	(30)	62		
	Vertical back porch	t_{VBP}	7	(9)	197	t_{HP}	
	Vertical front porch	t_{VFP}	2	(4)	97		
Data	Set up time	t_{SD}	5	-	-	ns	for DCLK
	Hold time	t_{HD}	10	-	-		
	Rise/Fall time	t_{Dr},t_{Df}	-	-	20	ns	

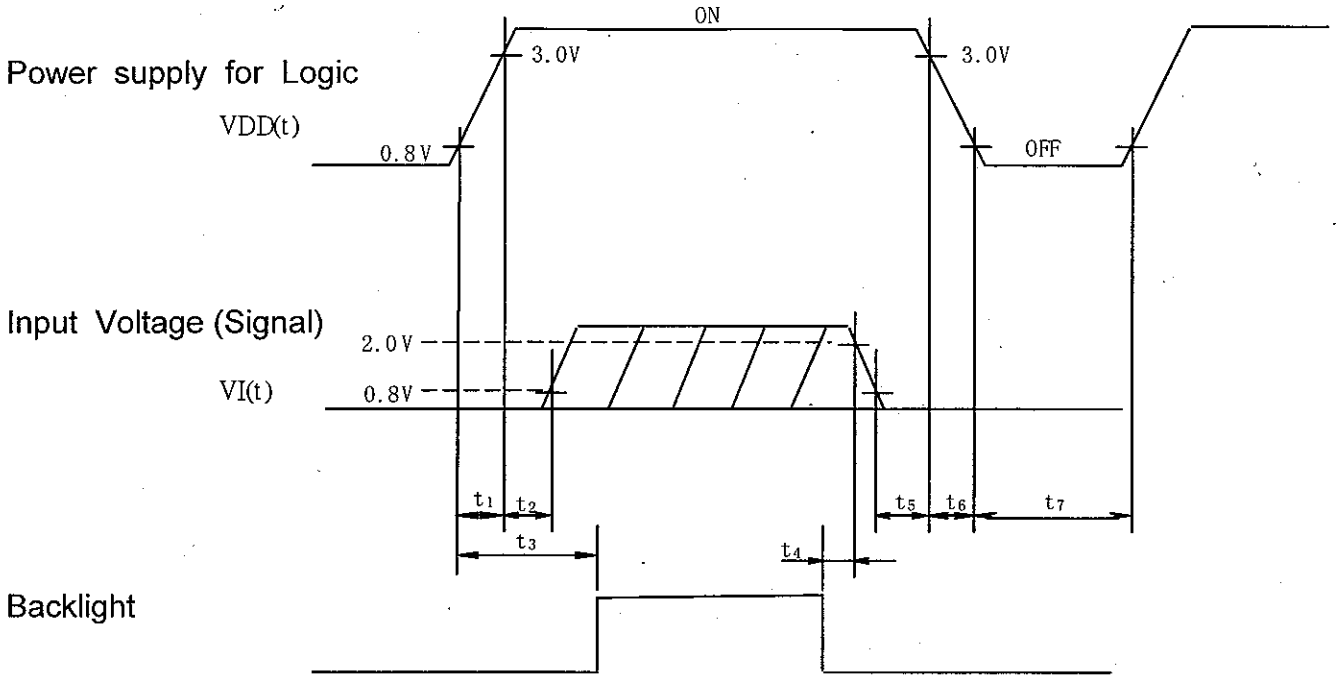
Note : Vsync Cycle should be set to odd.

8.2.2 INTERFACE TIMING FOR VGA DISPLAY MODE

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
DCLK	Cycle time	t_{CLK}	37.4	(47.8)	58.1	ns	
	Low level Width	t_{WCL}	15	-	-		
	High level Width	t_{WCH}	15	-	-		
	Rise time	t_{rCLK}	-	-	25		
	Fall time	t_{fCLK}	-	-	25		
	Duty	D	0.45	0.5	0.55	-	D= t_{CLKL}/ t_{CLK}
Hsync	Set up time	t_{SH}	5	-	-	ns	for DCLK
	Hold time	t_{HH}	10	-	-		
	Cycle	t_{HP}	679	(709)	739	tCLK	
	Valid width	t_{WH}	4	5	5		
	Rise/Fall time	t_{Hr},t_{Hf}	-	-	30	ns	
Vsync	Set up	t_{SV}	0	-	-	tCLK	for Hsync
	Hold	t_{HV}	2	-	-		
	Cycle	t_{VP}	485	(491)	533	tHP	
	Valid width	t_{WV}	2	2	2		
	Rise/Fall time	t_{Vr},t_{Vf}	-	-	50	ns	
DTMG	Set up time	t_{SI}	5	-	-	ns	for DCLK
	Hold time	t_{HI}	10	-	-		
	Rise/Fall time	t_{Ir},t_{If}	-	-	30	ns	
	Horizontal back porch	t_{HBP}	24	(37)	50	tCLK	
	Horizontal front porch	t_{HFP}	15	(32)	49		
	Vertical back porch	t_{VBP}	4	(7)	28	tHP	
	Vertical front porch	t_{VFP}	1	(4)	25		
Data	Set up time	t_{SD}	5	-	-	ns	for DCLK
	Hold time	t_{HD}	10	-	-		
	Rise/Fall time	t_{Dr},t_{Df}	-	-	25	ns	

Note : Vsync Cycle should be set to odd.

8.3 POWER ON/OFF SEQUENCE



POWER ON

$t_1 \leqq 15ms$

$0ms < t_2 \leqq 45ms$

$0.1s \leqq t_3$

POWER OFF

$5ms \leqq t_4$

$0ms \leqq t_5 \leqq 45ms$

$0ms \leqq t_6 \leqq 20ms$

$0.4s \leqq t_7$

Note 1 : $0V \leqq VI(t) \leqq VDD(t)$

VI(t) and VDD(t) is a surfeit of condition for power on/off.

Note 2 : Input Voltage(Signal) should not be set high impedance when power on.

8.4 RELATIONSHIP BETWEEN DISPLAYED COLOR AND INPUT DATA

	COLOR & GRAY SCALE	DATA SIGNAL																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

8.5 INTERNAL PIN CONNECTION

CN1 JAE : FA5B040HP1R3000(Au plating) (Suitable FPC : t0.3±0.03mm，0.5±0.03mm pitch)

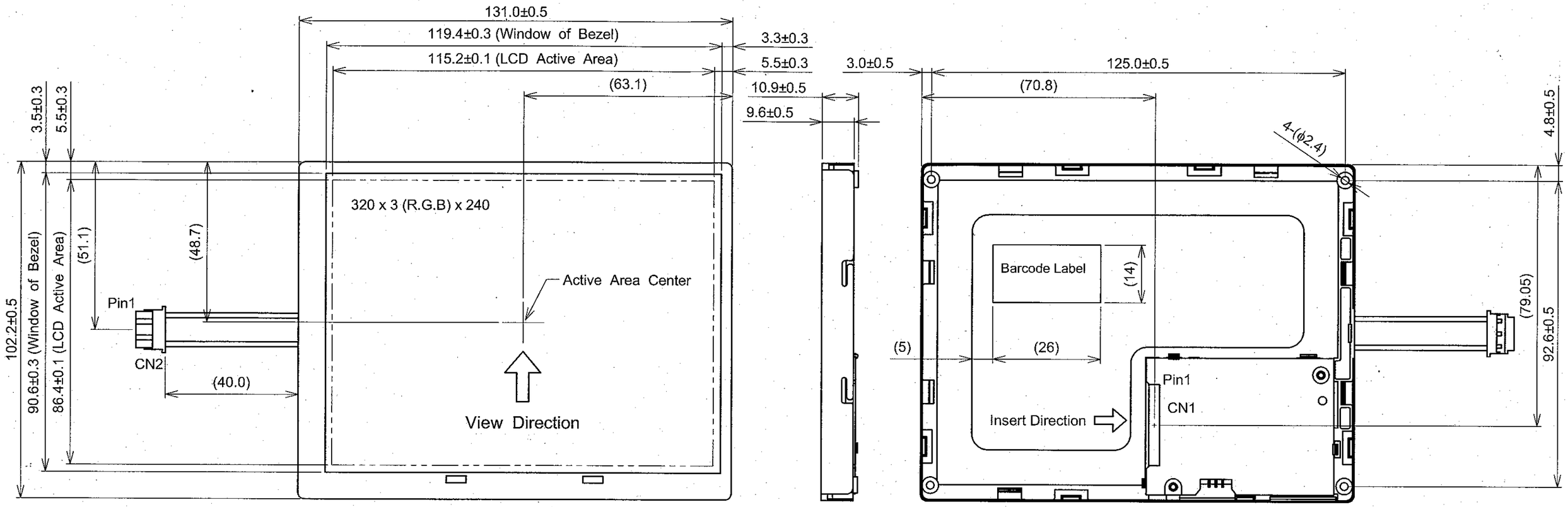
PIN No.	SIGNAL	FUNCTION
1	VDD	Power Supply for Logic
2	VDD	
3	VDD	
4	VDD	
5	NC	No Connection
6	DTMG	Timing Signal for Data
7	VSS	GND
8	DCLK	Dot Clock
9	VSS	GND
10	V/Q	Selection signal for VGA or QVGA ("H"=VGA，"L" or "NC" = QVGA)
11	VSS	GND
12	B5	Blue Data
13	B4	
14	B3	
15	VSS	GND
16	B2	Blue Data
17	B1	
18	B0	
19	VSS	GND
20	G5	Green Data
21	G4	
22	G3	
23	VSS	GND
24	G2	Green Data
25	G1	
26	G0	
27	VSS	GND
28	R5	Red Data
29	R4	
30	R3	
31	VSS	GND
32	R2	Red Data
33	R1	
34	R0	
35	TEST	(Note 1)
36	VSS	GND
37	NC	No Connection
38	NC	
39	NC	
40	NC	

Note 1 : Keep open electrically , HITACHI test only.

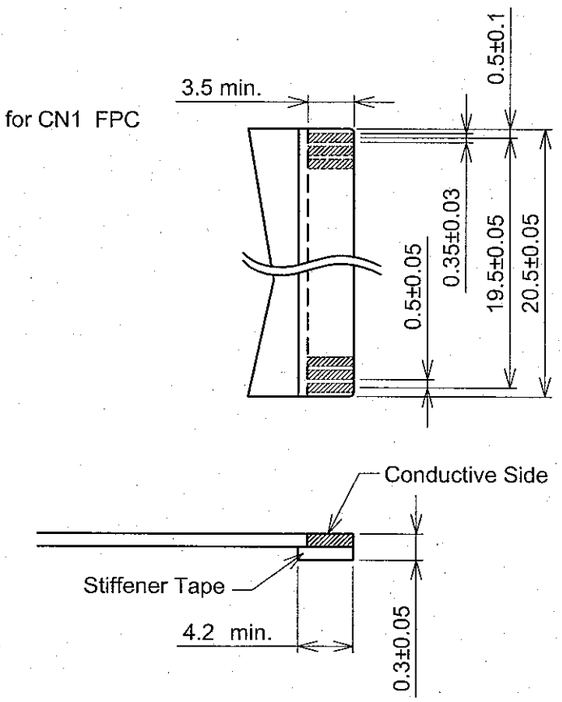
CN2 JST Housing : BHR-03VS-1

PIN No.	SIGNAL	LEVEL	FUNCTION
1	VL	-	Power Supply for CFL
2	NC	-	No connection
3	GND	-	GND for CFL(OV)

9. DIMENSIONAL OUTLINE



Recommended design rule for CN1 FPC



Scale : NTS
Unit : mm

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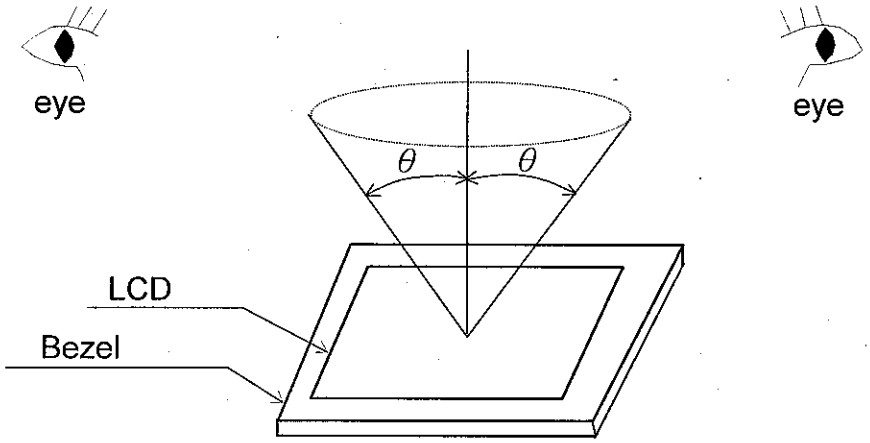
10. APPEARANCE STANDARD

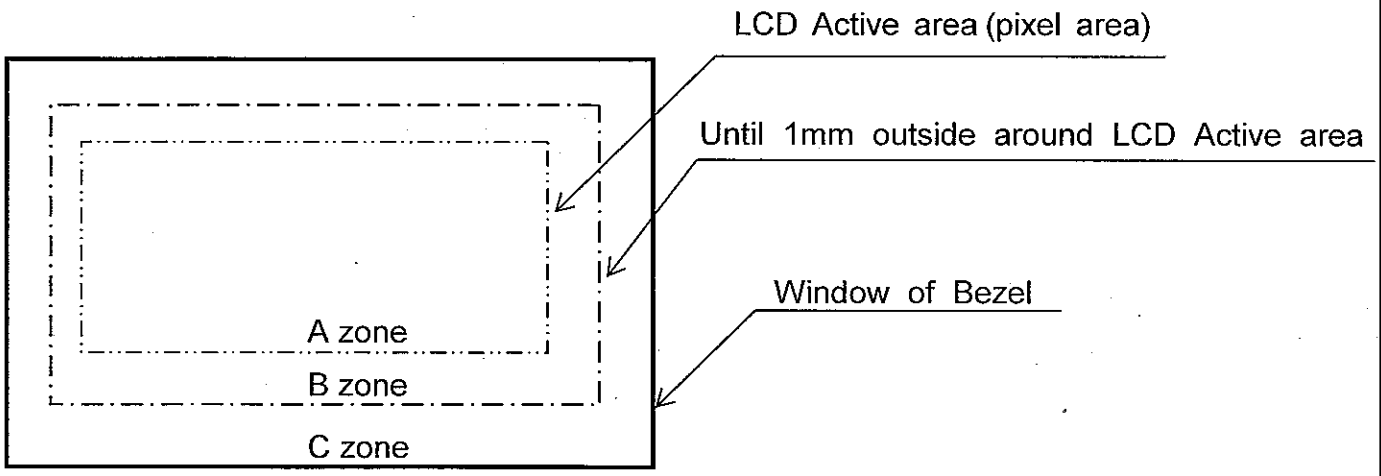
10.1 APPEARANCE INSPECTION CONDITION

Visual inspection should be done under the following condition.

(1) The inspection should be done in a dark room.
(about 1000(lx),500(lx)min. and non-directive)
(2) The distance between eyes of an inspector and the LCD module is 30cm.
(3) The viewing zone is shown the figure.
The θ is defined as $\theta \leqq 45^\circ$ for LCM power off
$\theta \leqq 5^\circ$ for LCM power on



10.2 DEFINITION OF ZONE



10.3 APPEARANCE SPECIFICATION

(1)LCD Appearance

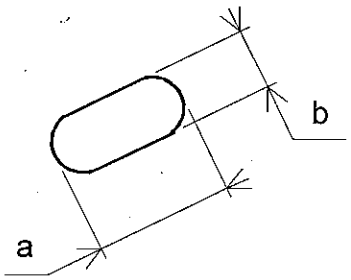
*) If the problem related to this section occurs about this item , the responsible persons of both party (Customer and HITACHI) will discuss the matter in detail.

No.	ITEM	CRITERIA				APPLIED ZONE
LCD	Scratches	Length L(mm)	Width W(mm)	Maximum number acceptable	Minimum space	A,B
		Ignored	W≦0.02	Ignored	-	
		L≦40	0.02<W≦0.04	10	-	
		L≦20	W≦0.04	10	-	
	Dent	Distinguished one is acceptable (To be judged by HITACHI standard)				A
	Wrinkles in Polarizer	Same as above				A
	Bubbles	Average diameter D(mm)		Maximum number acceptable		A
		D≦0.2		Ignored		
		0.2<D≦0.3		12		
		0.3<D≦0.5		3		
		0.5<D		none		
	Stains Foreign Materials Dark Spot	Filamentous (Line shape)				A,B
		Length L(mm)	Width W(mm)	Maximum number acceptable		
		L≦2.0	W≦0.03	Ignored		
		L≦3.0	0.03<W≦0.05	6		
		L≦2.5	0.05<W≦0.1	1		
		Round(Dot shape)				A,B
		Average diameter D(mm)	Maximum number acceptable	Minimum Space		
		D<0.2	Ignored	-		
		0.2≦D<0.3	10	10 mm		
		0.3≦D<0.4	5	30 mm		
		0.4≦D	none	-		
		The total number	Filamentous + Round=10			
		Those wiped out easily are acceptable				
	Color Tone	To be judged by HITACHI STANDARD				A
	Color Uniformity	Same as above				A
	Dot Defect			Maximum number acceptable		A
		Sparkle mode	1 dot	4		
			2 dots (Note.(3)-(f))	1		
			Total	5		
		Black mode	1 dot	5		
			2 dots (Note.(3)-(f))	2		
			Total	5		
			Total	10		

(2) CFL BACKLIGHT APPEARANCE

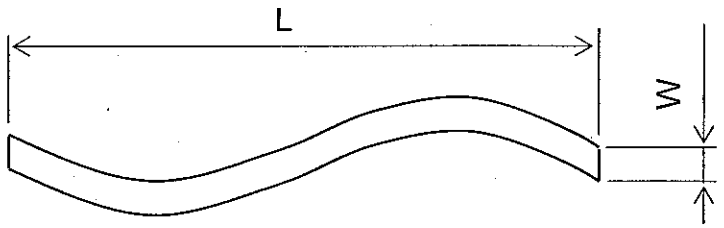
No.	ITEM	CRITERIA			APPLIED ZONE
CFL BACKLIGHT	Dark Spots White Spots Foreign Materials (Spot)	Average diameter D(mm)		Maximum number acceptable	A
		D≦0.4		ignored	
		0.4＜D		none	
	Foreign Materials (Line)	Width W(mm)	Length L(mm)	Maximum number acceptable	A
		W≦0.2	L≦2.5	1	
			2.5＜L	None	
		0.2<W	-	none	
	Scratches	Width W(mm)	Length L(mm)	Maximum number acceptable	A
		W≦0.1	-	ignored	
		0.1＜W≦0.2	L≦11.0	1	
			11.0＜L	None	
		0.2＜W	-	none	

Note 1 : Definition of average diameter (D)



$$D=\frac{a+b}{2}$$

Note 2 : Definition of length (L) and width (W)



Note 3 : Definition of dot defect

(a) Dot Defect : Defect Area $>$ 1/2 dot

(b) Sparkle mode : Brightness of dot is more than 30% at Black raster.

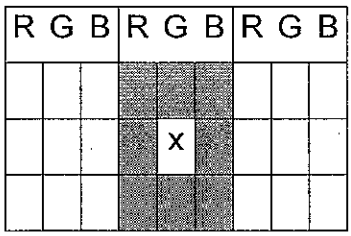
(c) Black mode : Brightness of dot is less than 70% at R.G.B raster.

(d) 1 dot : Defect dot is isolated , not attached to other defect dot.

(e) N dot : N defect dots are consecutive (fig.1).

(N means the number of defect dots.)

(fig .1)



2 dots defect included defect dot "X" is defined as follows.

Adjacent dots to defect dot "X" :

(f) Counting definition of adjacent dots (1 set) : same as 1 dot defect.

(g) Those wiped out easily are acceptable.

11. PRECAUTION IN DESIG

11.1 PRECAUTIONS AGAINST ELECTROSTATIC DISCHARGE

As this module contains C-MOS LSIs, it is not strong against electrostatic discharge. Make certain that the operator's body is connected to the ground through a list band , etc. And don't touch I/F pins directly.

11.2 HANDLING PRECAUTIONS

(1) As the adhesives used for adhering upper/lower polarizer's and frame are made of organic substances which will be deteriorated by a chemical reaction with such chemicals as acetone, toluene, ethanol and isopropyl alcohol. The following are recommended for use :
normal hexane
Please contact with us when it is necessary for you to use chemicals other than the above.

(2) Lightly wipe to clean the dirty surface with absorbent cotton or other soft material like chamois, soaked in the recommended chemicals without scrubbing it hardly. Always wipe the surface horizontally or vertically. Never give a wipe in a circle. To prevent the display surface from damage and keep the appearance in good state, it is sufficient, in general, to wipe it with absorbent cotton.

(3) Immediately wipe off saliva or water drop attached on the display area because it may cause deformation or faded color.

(4) Fogy dew deposited on the surface may cause a damage, stain or dirt to the polarizer.
When you need to take out the LCD module from some place at low temperature for test, etc.
It is required to be warmed them up to temperature higher than room temperature before taking them out.

(5) Touching the display area or I/F pins with bare hands or contaminating them are prohibited, because the stain on the display area and poor insulation between terminals are often caused by being touched with bare hands.
(Some cosmetics are detrimental to polarizer's.)

(6) In general, the glass is fragile so that, especially on its periphery, tends to be cracked or chipped in handling. Please not give the LCD module sharp shocks by falling, etc.

(7) Maximum pressure to the surface must be less than 1.96×10^4 Pa.
And if the pressure area is less than $1cm^2$, maximum pressure must be less than 1.96N.

(8) Since the metal width is narrow on these locations (see page 9-1/1), please careful with handling.

(9) Top sheets shall be cleaned gently using a soft cloth such as those used for glasses. Hard wiping accumulated dust will leave scars on the surface even using a cloth.

11.3 OPERATION PRECAUTION

(1) Using a LCM module beyond its maximum ratings may result in its permanent destruction.
LCM module's should usually be used under recommended operating conditions shown in chapter 4. Exceeding any of these conditions may adversely affect its reliability.

(2) Response time will be extremely delayed at lower temperature than the specified operating temperature range and on the other hand LCD's shows dark blue at higher temperature.
However those phenomena do not main defects of the LCD module. Those phenomena will disappear in the specified operating temperature range.

(3) If the display area is pushed hard during operation, some display patterns will be abnormally display.

(4) A slight dew depositing on terminals may cause electrochemical reaction which leads to terminal open circuit. Please operate the LCD module under the relative condition of 40℃ 85%RH.

11.4 STORAGE

In case of storing LCD module for a long period of time (for instance, for years) for the purpose of replacement use, the following precautions necessary.

(1) Store the LCD modules in a dark place; do not expose them to sunlight or ultraviolet rays.

(2) Keep the temperature between 10℃ and 35℃ at normal humidity.

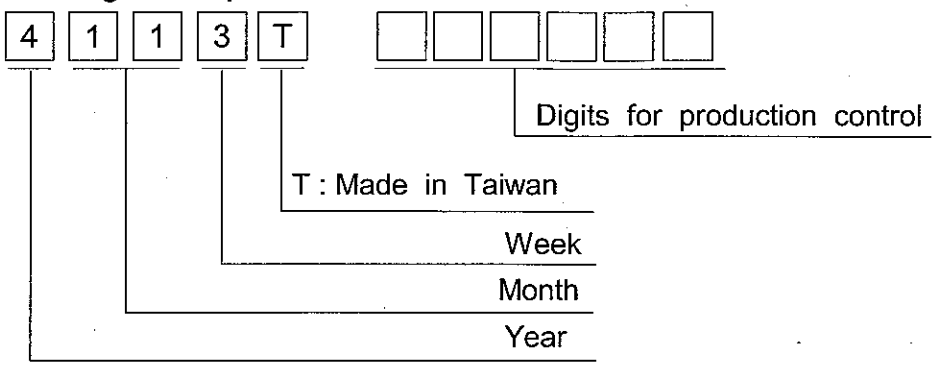
(3) Store the LCD modules in the container which is used for shipping from us.

(4) No articles shall be left on the surface over an extended period of time.

12. DESIGNATION OF LOT MARK

12.1 LOT MARK

Lot mark is consisted of 5 digits for production lot and 6 digits for production control.



Year	Figure in lot mark
2008	8
2009	9
2010	0
2011	1
2012	2

Month	Figure in lot mark	Month	Figure in lot mark
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sep.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week (day in calendar)	Figure in lot mark
1~ 7	1
8~14	2
15~21	3
22~28	4
29~31	5

12.2 SERIAL No.

Serial No. is consisted of 6 digits number (000001~999999).

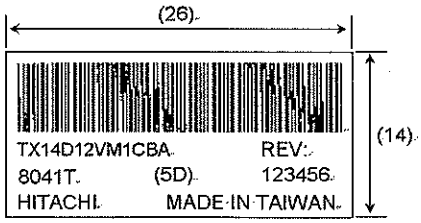
12.3 LOCATION OF LOT MARK

Label is bring attached on the back side of module.

12.4 REVISION(Rev.) CONTROL

Rev. column is controlled by the manufacturing A-Z expect I and 0 is to be written on this column

Rev No.	ITEM
A	PCB for QVGA Display Mode
B	PCB for QVGA&VGA Display Mode (H : VGA ; L or NC : QVGA)
C	CN1 JAE : FA5B040HP1R3000



13. PRECAUTION FOR USE

(1) A limit sample should be provided by the both parities on an occasion when the both parties agree to its necessity.
Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

(2) On the following occasions, the handling of the problem should be decided through discussion and agreement between responsible persons of the both parties.

(1) When a question is arisen in the specifications.

(2) When a new problem is arisen which is not specified in this specifications.

(3) When an inspection specifications change or operating condition change by customer is reported to HITACHI, and some problem is arisen in the specification due to the change.

(4) When a new problem is arisen at the customer's operating set for sample evaluation.

(3) Regarding the treatment for maintenance and repairing, both parties will discuss it in six months later after latest delivery of this product.

The precaution that should be observed when handling LCM have been explained above.
If any points are unclear or if you have any requests , please contact with HITACHI.