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Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(V) Final Specifications

Module	14.1" WXGA Color TFT-LCD with LED Backlight design
Model Name	B141EW05 V1
Note ()	<i>LED Backlight with driving circuit design</i>

Customer	Date
Checked & Approved by	Date
<p>Note: This Specification is subject to change without notice.</p>	

Approved by	Date
Prepared by	
<p>NBBU Marketing Division / AU Optronics corporation</p>	



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2007/10/25	All	First Edition for Customer		
0.2 2007/12/12	16 28,29 18,19 5 13 33	Modify (1) Pixel Format Image (2) LCM Outline drawing (3) Pin assignment (4) Power Consumption (5) Logic Power Consumption (6) EDID code	(1) Modify RGB orders (2) Modify connector position (3) Modify Pin assignment 30~40 (4) Total Power Consumption=4.9W (5) Logic Power Consumption=1.1W (6) Update EDID code	
0.3 2008/1/11	18	Update (1)Pin assigment	(1) Update Pin assigment	
0.4 2008/2/18	5	Update (1) Brightness spec.	(1) Brightness typ. 220 min.187	
0.5 2008/2/27	5	Power consumption to 4.9W(max)	Total Power consumption <4.2W excluded the conversion efficiency	
0.6 2008/3/12	24	LED Power ON/OFF Sequence	Add Panel Power ON/OFF Sequence	
0.7 2008/4/14	27	Vibration test Spec. Frequency: 5~150 Hz	Vibration test Spec. Frequency: 10~500 Hz	
0.8 2008/5/20	28	Drawing	Update drawing	
0.9 2008/5/21	26	Mating Housing/Part Number	IPEX 20345 series or compatible	
1.0 2008/8/12	6,22	RGB Chromaticity Coodinates Clock frequency	RGB Chromaticity Coodinates Clock frequency=71.1	
1.1 200810/02	15	Output PWM frequency=200 HzMax Duty ratio =20% Min	Output PWM frequency=20K HzMax Duty ratio =15% Min	
	32	Update EDID	Update EDID	

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. High voltage is supplied to these parts when power turn on.



2. General Description

B141EW05 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B141EW05 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	357.7 (14.1W")			
Active Area	[mm]	303.36 X 189.6			
Pixels H x V		1280x3(RGB) x 800			
Pixel Pitch	[mm]	0.237			
Pixel Format		B.G.R. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I _{LED} =20mA) Note: I _{LED} is LED current	[cd/m ²]	220 typ. (5 points average) 187 min. (5 points average) (Note1)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 12 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.2 max. (Include Logic and Blu power) (Note1)			
Weight	[Grams]	375 max.			
Physical Size without inverter, bracket.	[mm]		Min.	Typ.	Max.
		Length	319	319.5	320
		Width	205	205.5	206
		Thickness	4.8	-	5.5
Electrical Interface		1 channel LVDS			
Surface Treatment		Anti-Glare,			



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Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +65
RoHS Compliance		RoHS Compliance

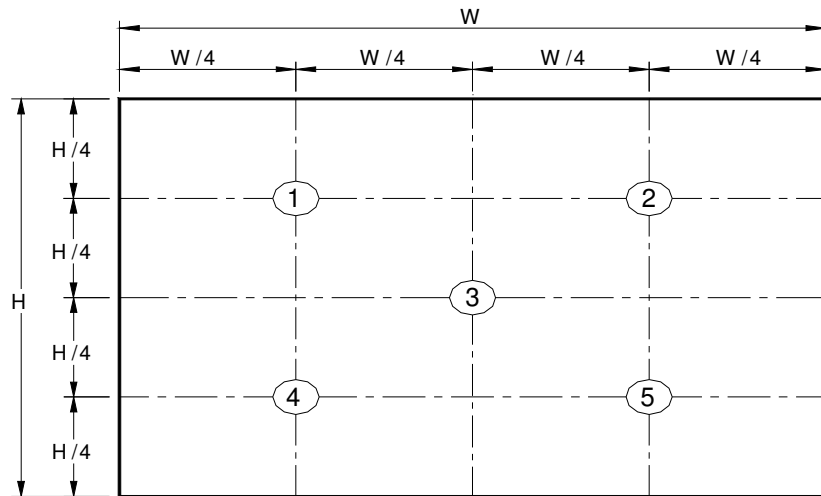
Note 1. Total power consumption including LED power efficiency <4.9W max.

2.2 Optical Characteristics

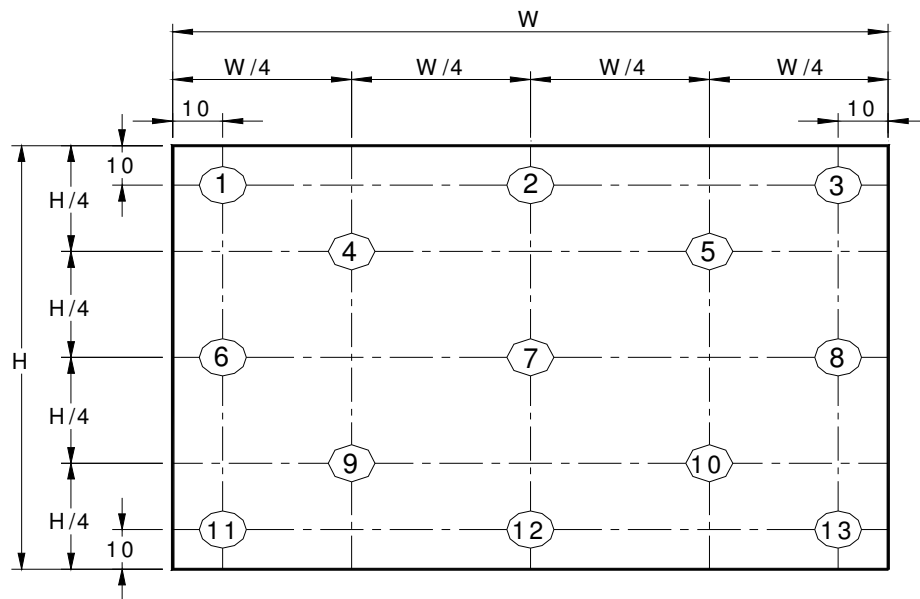
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I _{LED} =20mA		5 points average	187	220	-	cd/m ²	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right) CR = 10 (Left)	40	45	-	degree	4, 9
	θ_L		40	45	-		
	ϕ_H	Vertical (Upper) CR = 10 (Lower)	10	15	-		
	ϕ_L		30	35	-		
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio	CR		300	400	-		4, 6
Cross talk	%				4		4, 7
Response Time	T _r	Rising	-	6	10	msec	4, 8
	T _f	Falling	-	2	5-		
	T _{RT}	Rising + Falling	-	8	12		
Color / Chromaticity Coordinates NTSC	Red x	CIE 1931	0.525	0.575	0.625		4
	Red y		0.285	0.335	0.385		
	Green x		0.265	0.315	0.365		
	Green y		0.500	0.550	0.600		
	Blue x		0.105	0.155	0.205		
	Blue y		0.085	0.135	0.185		
	White x		0.263	0.313	0.363		
	White y		0.279	0.329	0.379		
%	-	45	-				

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



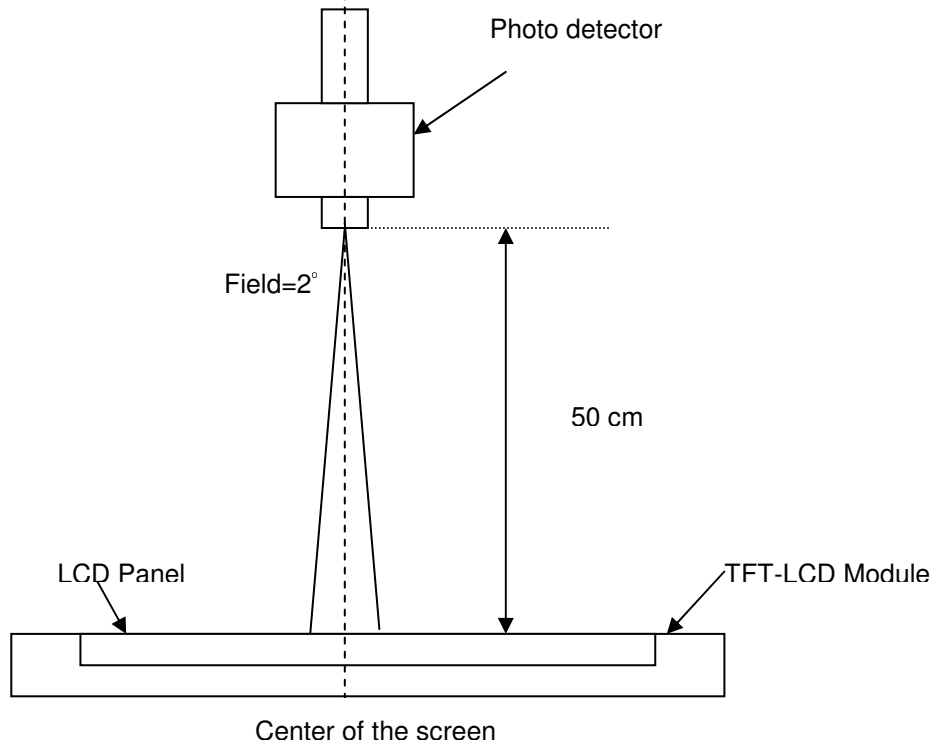
Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, , and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

$L (x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

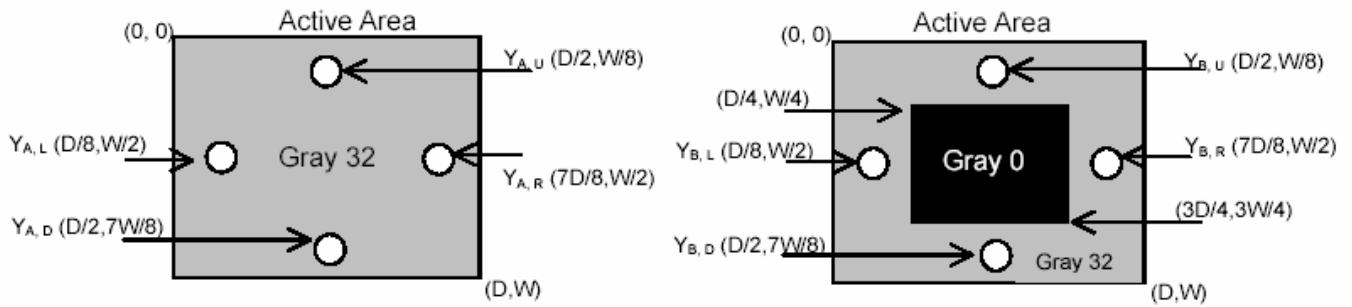
Note 7 : Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

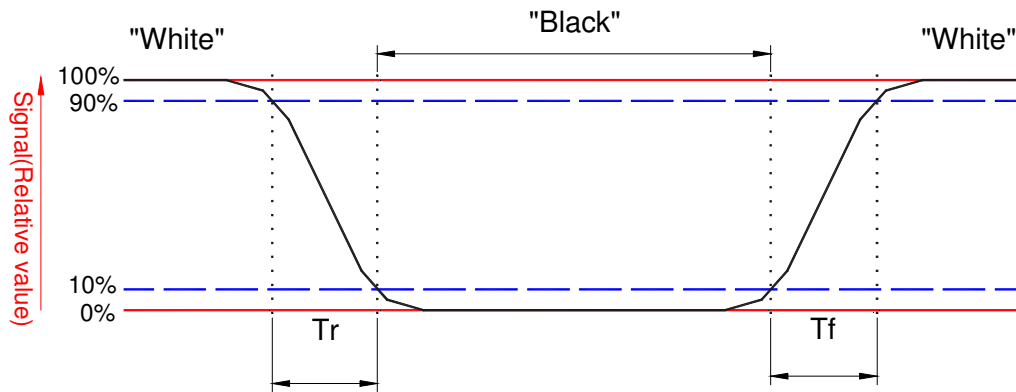
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



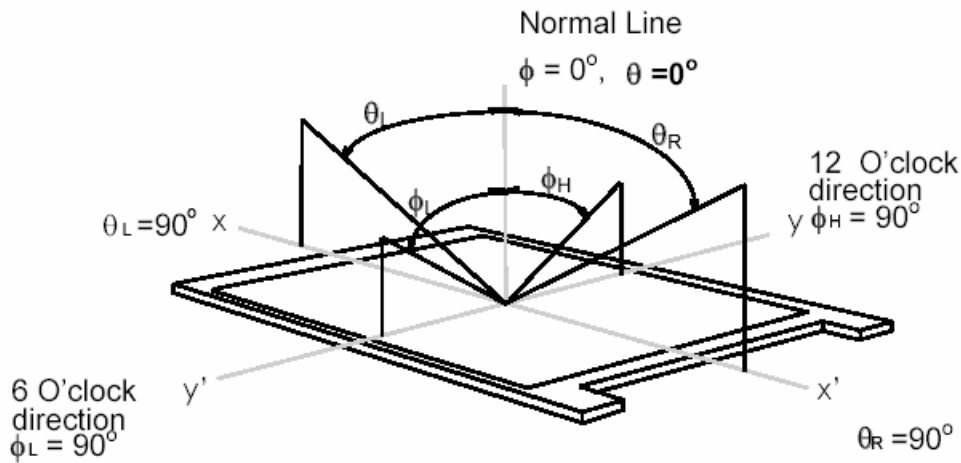
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



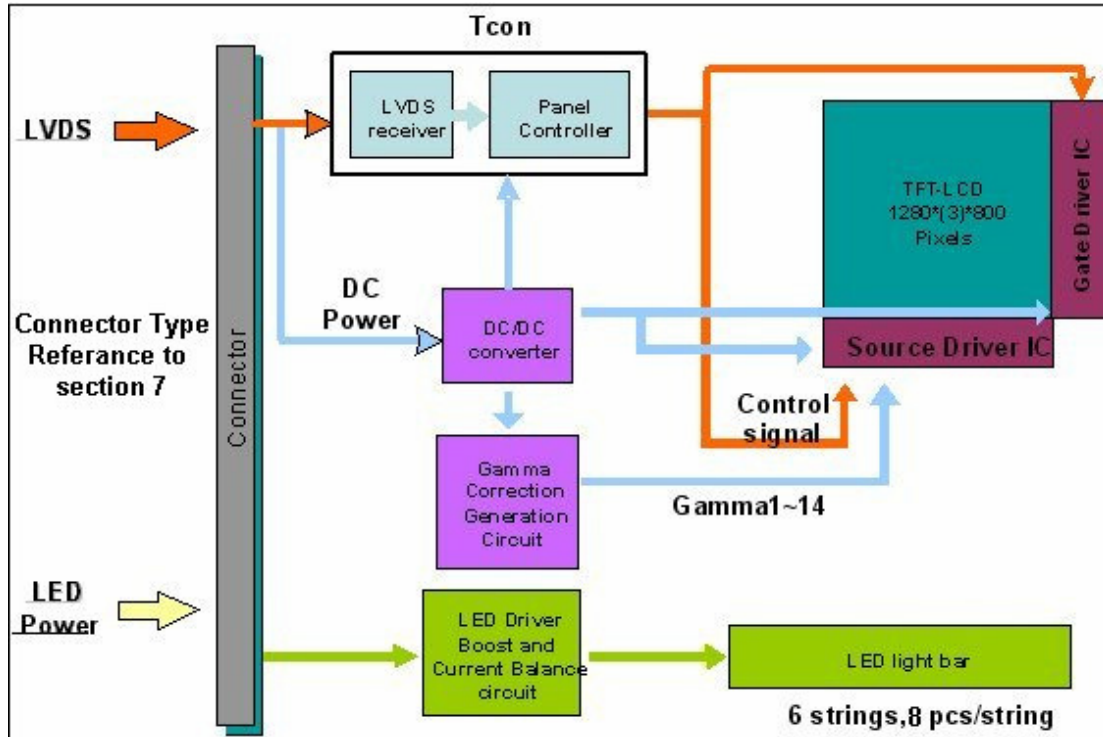
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches wide Color TFT/LCD 40 Pin (One ch/connector Module):



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V _{in}	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
LED Driving Voltage	V _{LED}	-	36 (Row Output)	[Volt]	Note 1,2,3
LED Driving Current	I _{LED}	-	30 (Row Output)	[mA] rms	Note 1,2,3

4.3 Absolute Ratings of Environment

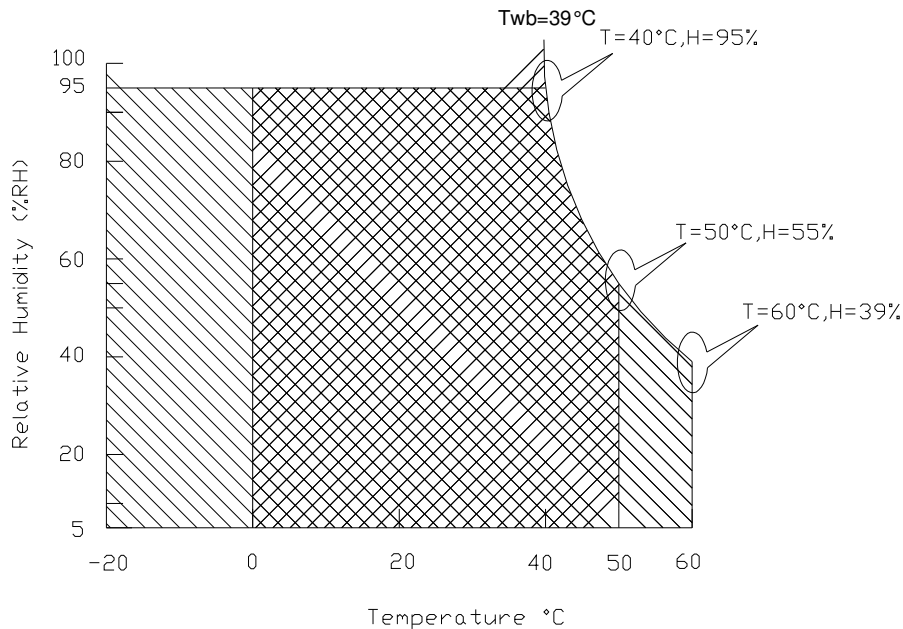
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	8	95	[%RH]	Note 4
Storage Temperature	TST	-20	+65	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

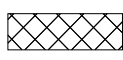
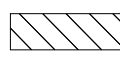
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

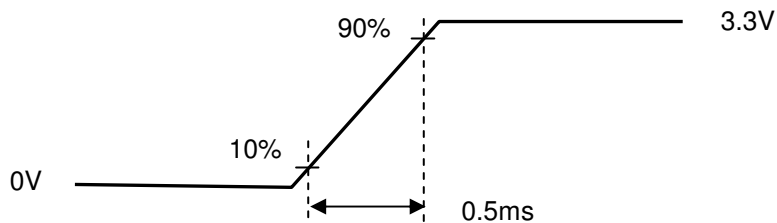
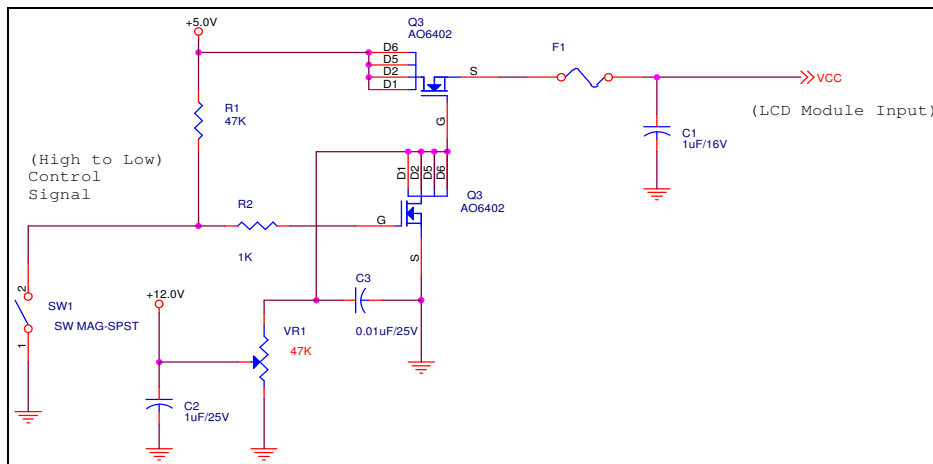
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.1	[Watt]	Note 1/2
IDD	IDD Current	-	350	450	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



Vin rising time

5.1.2 Signal Electrical Characteristics

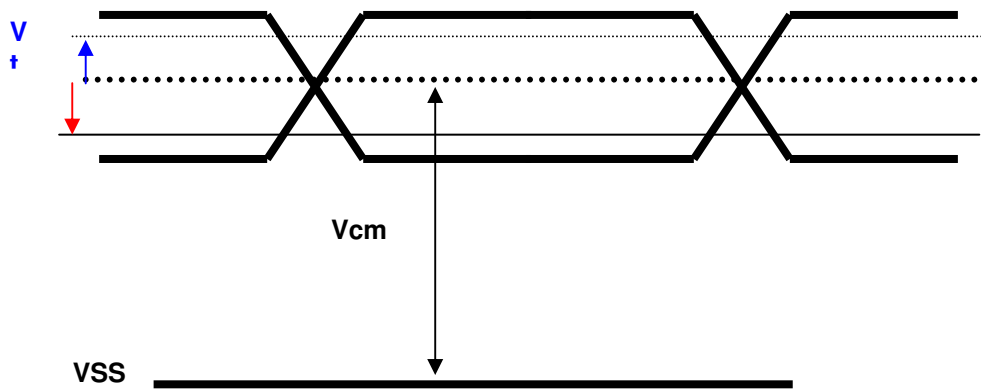
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

LED Parameter guideline for LED driving selection (Ref. Remark 1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	V_F	2.95	3.15	3.35	[Volt]	($T_a=25^\circ\text{C}$)
LED Forward Current	I_F		20	30	[mA]	($T_a=25^\circ\text{C}$)
LED Power consumption	P_{LED}		3.78		[Watt]	($T_a=25^\circ\text{C}$) Note 1
LED Life-Time	N/A	10,000	-	-	Hour	($T_a=25^\circ\text{C}$) $I_F=20\text{ mA}$ Note 2
Output PWM frequency	F_{PWM}	180	200	20K	Hz	
Duty ratio	--	15	--	100	%	

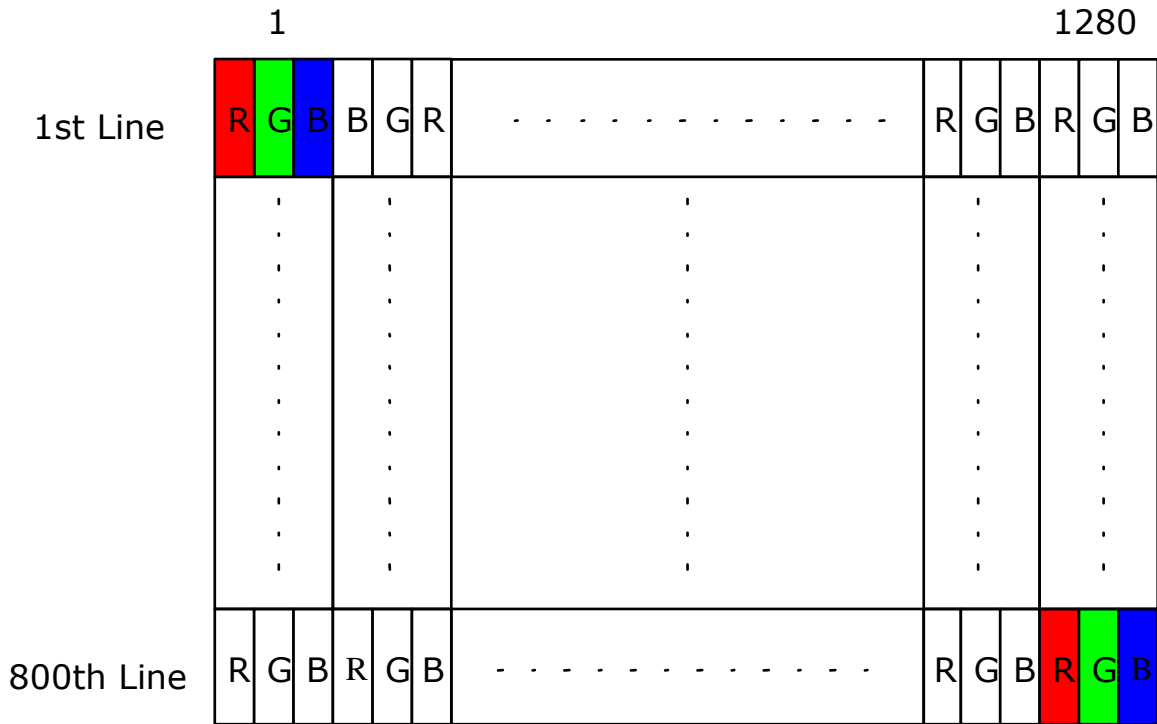
Note 1: Calculator value for reference $I_F \times V_F = P$

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

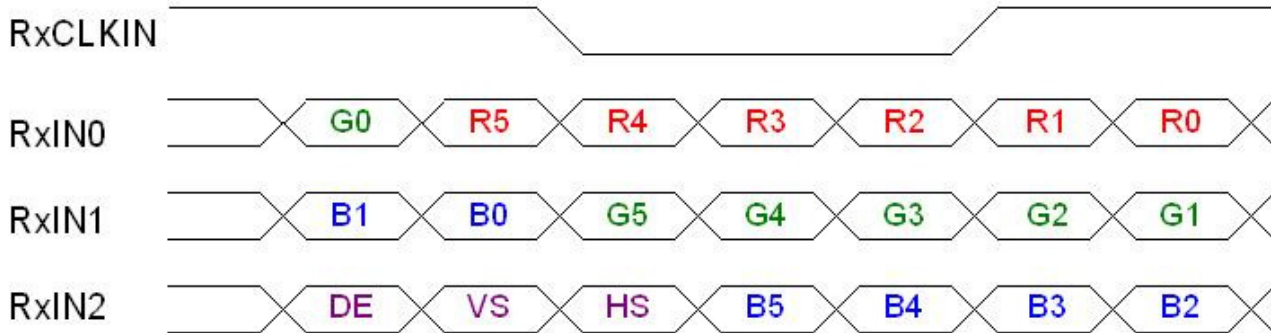
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V _{EDID}	+3.3V EDID Power
5	NC	No Connection (Reserve for AUO test)
6	CLK _{EDID}	EDID Clock Input
7	DATA _{EDID}	EDID Data Input
8	RxIN0-	LVDS differential data input(R0-R5, G0)
9	RxIN0+	LVDS differential data input(R0-R5, G0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(G1-G5, B0-B1)
12	RxIN1+	LVDS differential data input(G1-G5, B0-B1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(B2-B5, HS, VS, DE)
15	RxIN2+	LVDS differential data input(B2-B5, HS, VS, DE)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	NC	No Connection (Reserve for AUO test)

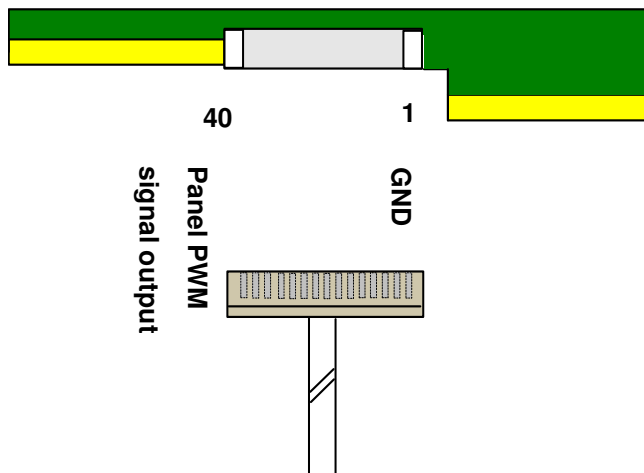
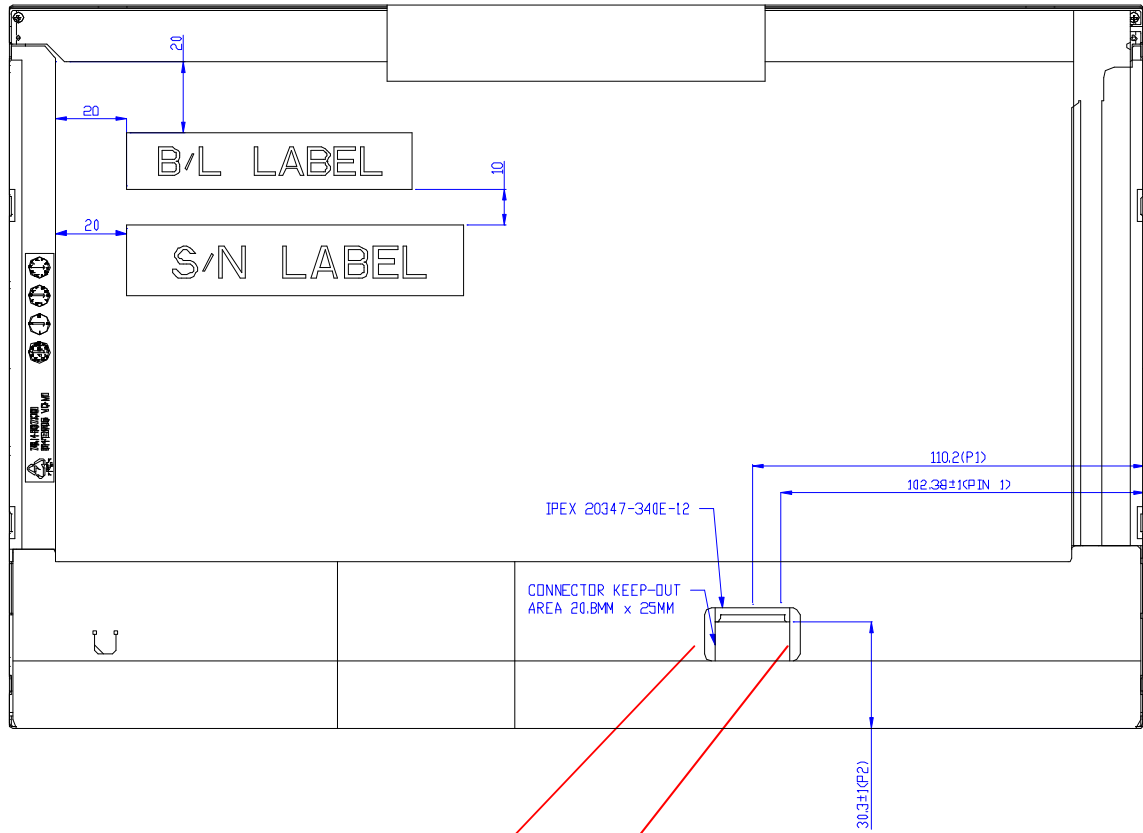


Product Specification

AU OPTRONICS CORPORATION

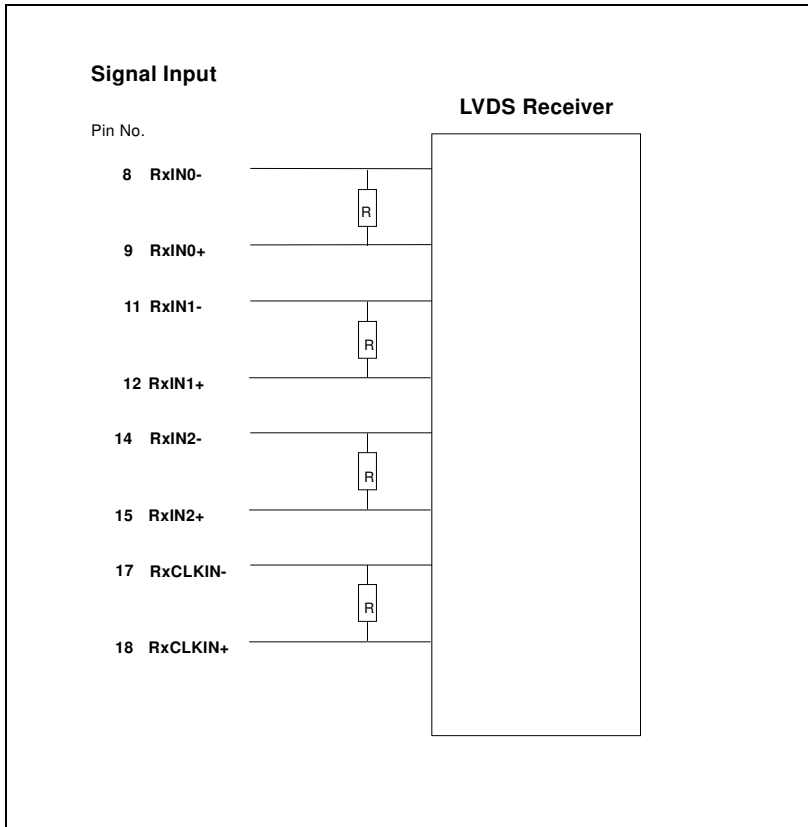
PIN#	Signal Name	Description
21	NC	No Connection (Reserve for AUO test)
22	GND	Ground
23	NC	No Connection (Reserve for AUO test)
24	NC	No Connection (Reserve for AUO test)
25	GND	Ground
26	NC	No Connection (Reserve for AUO test)
27	NC	No Connection (Reserve for AUO test)
28	GND	Ground
29	NC	No Connection (Reserve for AUO test)
30	NC	No Connection (Reserve for AUO test)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	VLED	LED Power Supply 7V-20V
35	VLED	LED Power Supply 7V-20V
36	VLED	LED Power Supply 7V-20V
37	VLED	LED Power Supply 7V-20V
38	S_PWMIN	System PWM signal Input
39	LED_EN	LED enable pin (+3V input)
40	NC	NC

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.
 internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

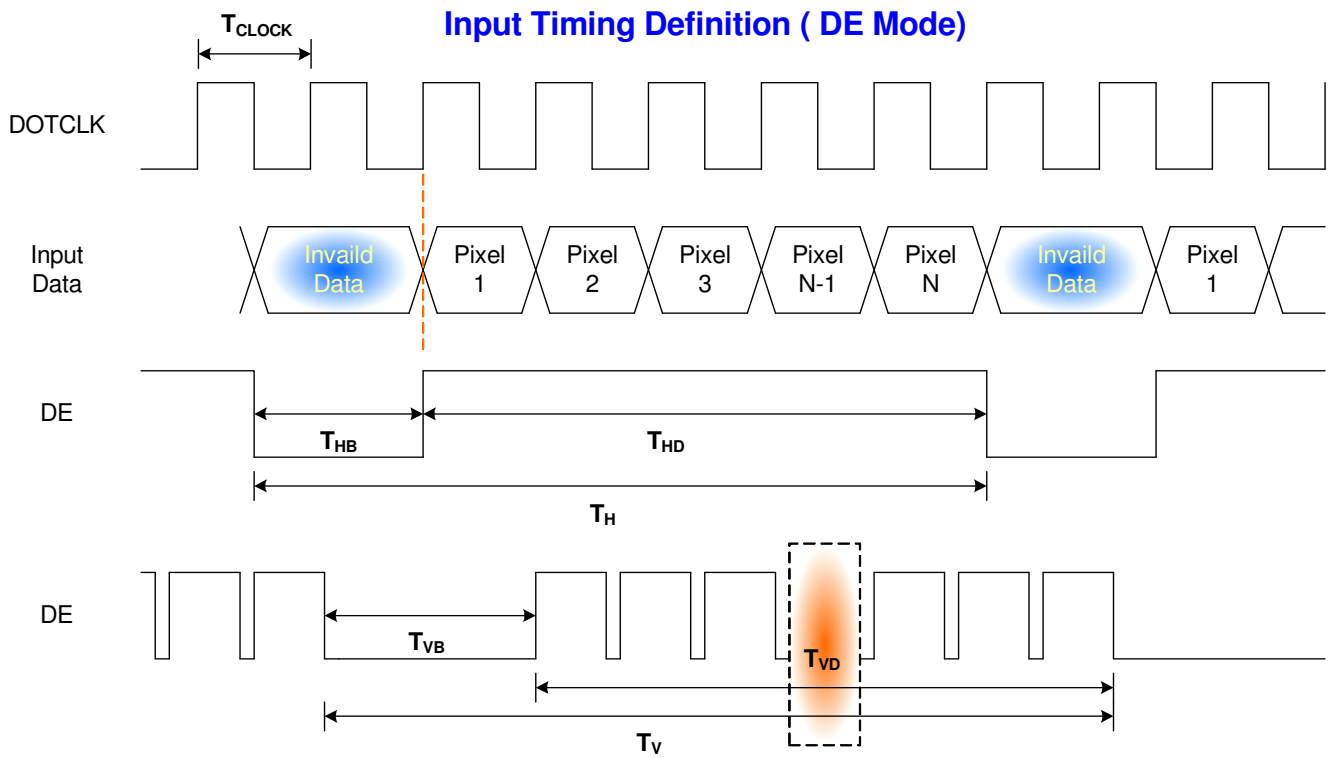
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	-	60	-	Hz	
Clock frequency	$1/T_{\text{Clock}}$	-	71.1	-	MHz	
Vertical Section	Period	T_V	803	816	1023	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	223	
Horizontal Section	Period	T_H	1303	1408	2047	T_{Clock}
	Active	T_{HD}	1280	1280	1280	
	Blanking	T_{HB}	23	118	767	

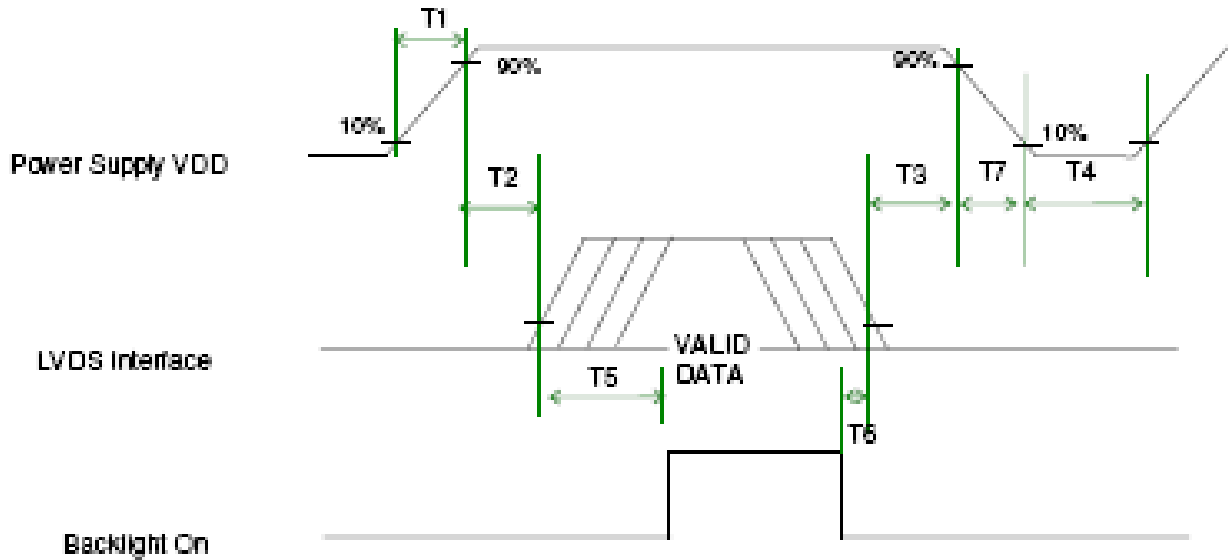
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

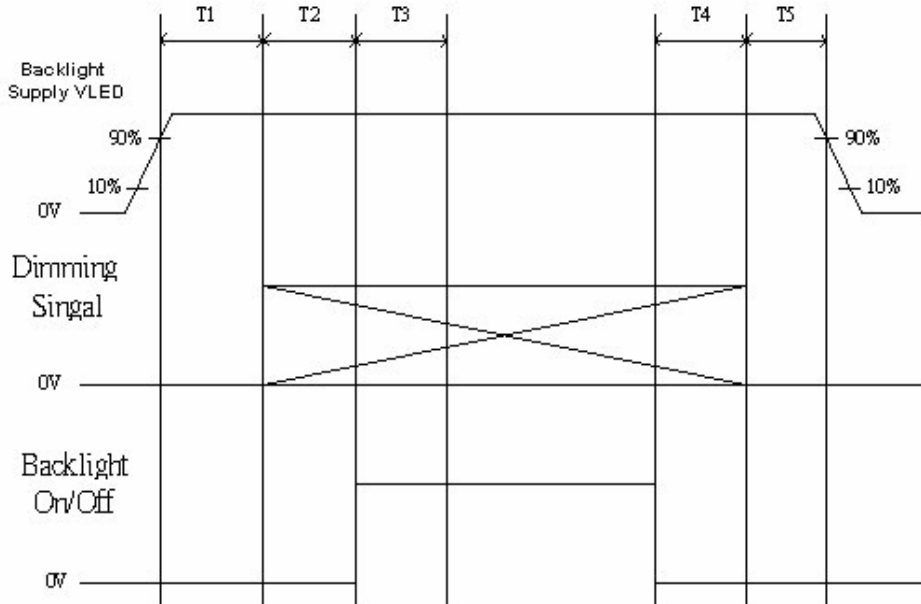
VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

LED on/off sequence is as follows. Interface signals are also shown in the chart.



Power Sequence Timing

Symbol	Value			Unit
	Min	Typ	Max	
T1	10	---	---	ms
T2	10	---	---	ms
T3	50	---	---	ms
T4	0	---	---	ms
T5	10	---	---	ms

Note: The duty of LED dimming signal should be more than 20% in T2 and T3.

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20347-340E-12 or compatible
Mating Housing/Part Number	IPEX 20345 series or compatible

8. LED Driving Specification

8.1 Connector Description

It is a integrative interface and comibe into LVDS connector. The type and mating refer to section 7.

8.2 Pin Assignment

Ref. to 6.3

9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G , Half sine pulse
- Frequency: 10 - 500Hz Sine wave
- Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 240 G , Half sine pulse
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side



10. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 300h	
Low Temperature Storage	Ta= -20°C, 300h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
. Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

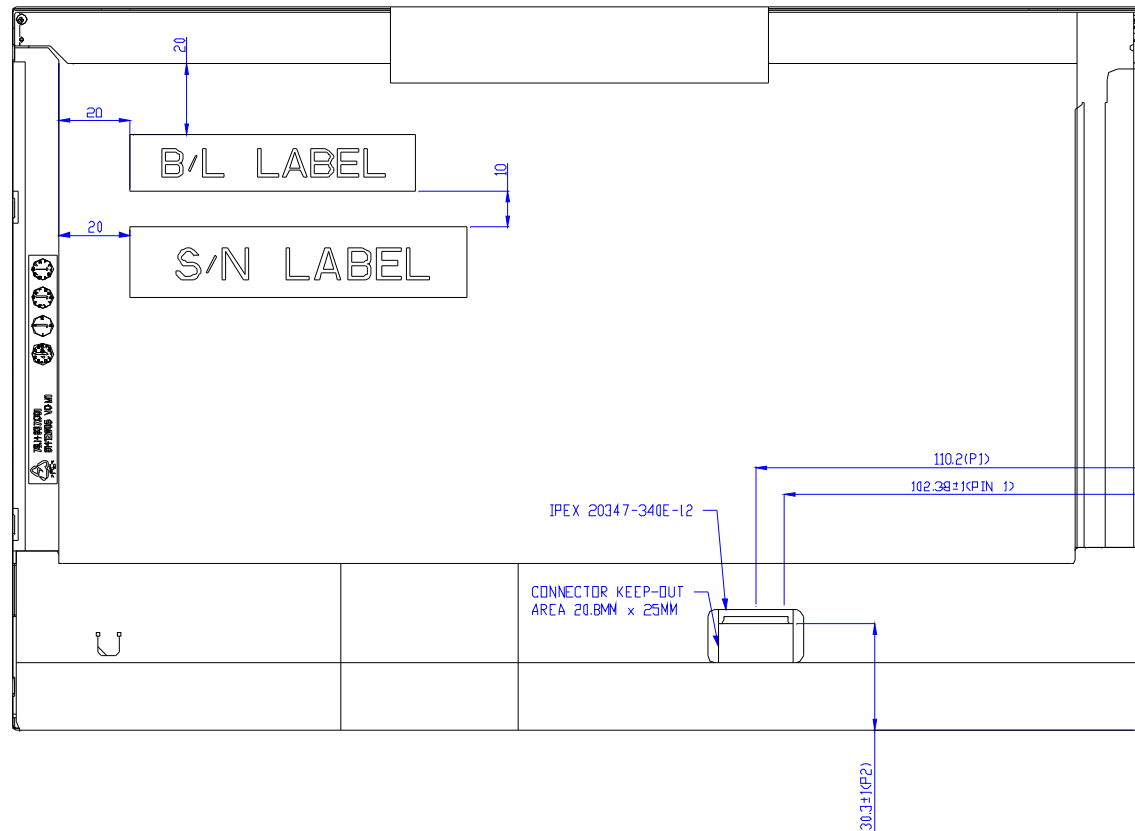


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11. Mechanical Characteristics

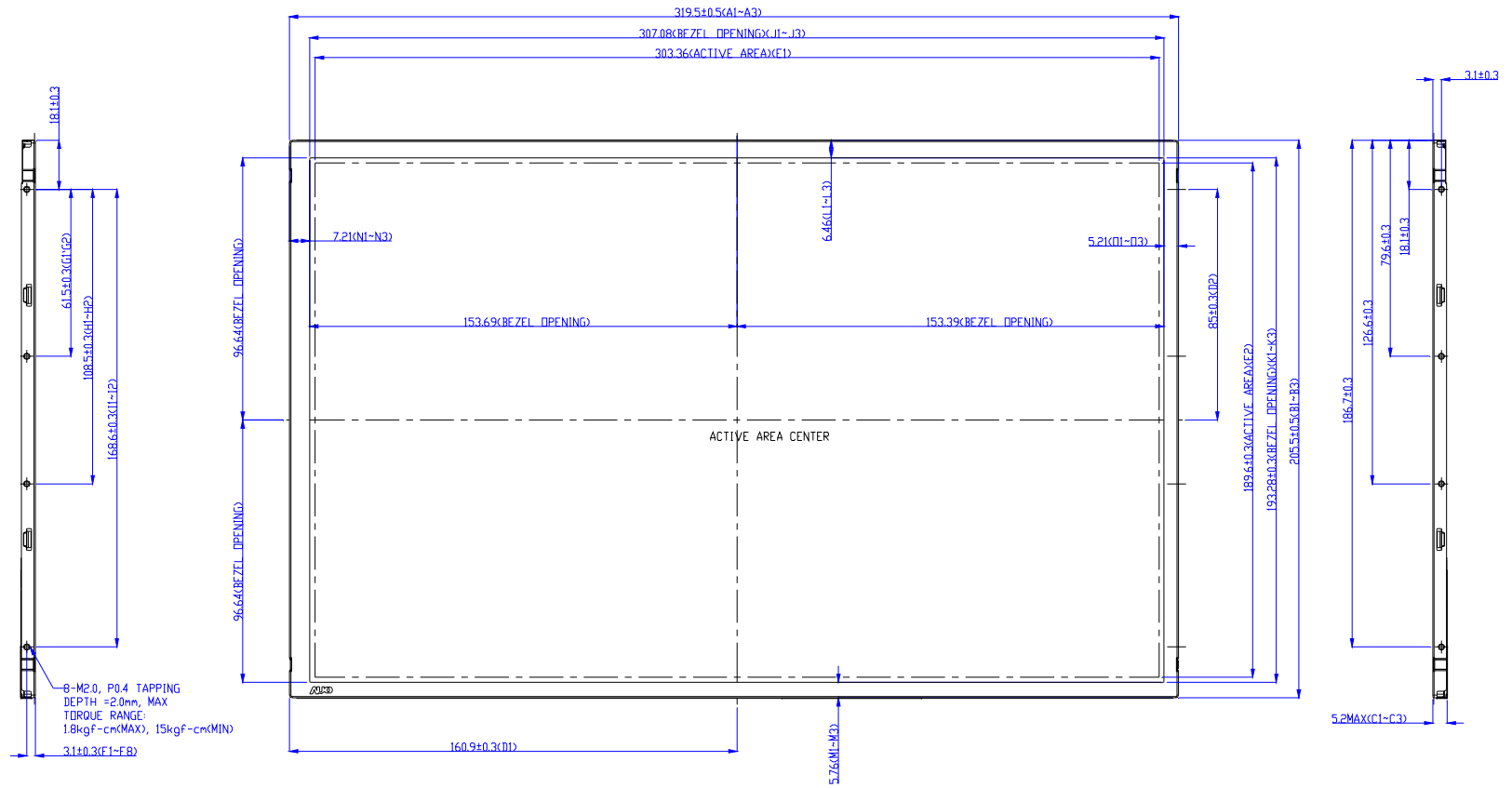
11.1 LCM Outline Dimension





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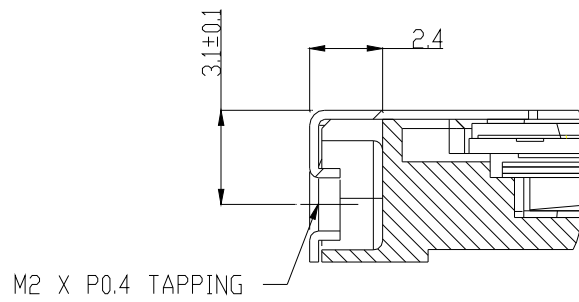


11.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.1 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.2 mm (See drawing)

Screw Torque: Maximum 2.5 kgf-cm



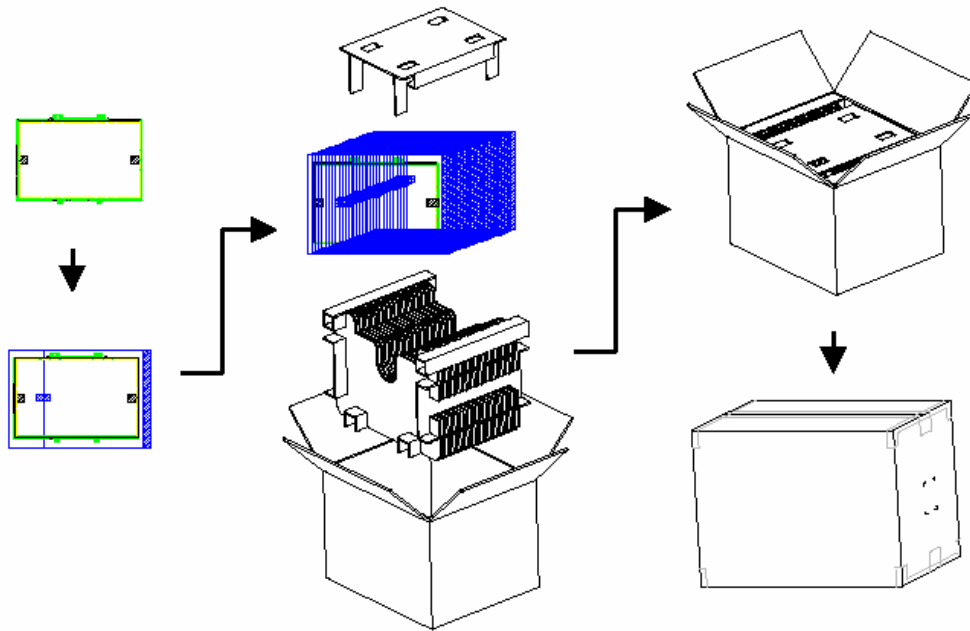
12. Shipping and Package

12.1 Shipping Label Format

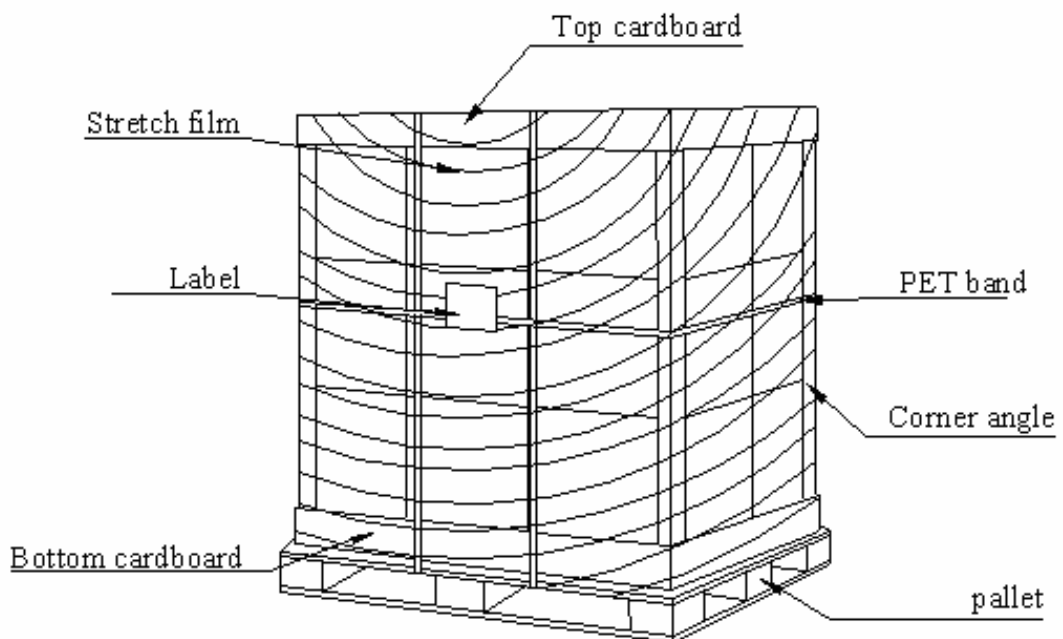


12.2 Carton package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm



11.3 Shipping package of palletizing sequence





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13. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	44	01000100	68	
0B	hex, LSB first	51	01010001	81	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	11	00010001	17	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	Video input def. (<i>digital I/P, non-TMDS, CRGB</i>)	80	10000000	128	
15	Max H image size (<i>rounded to cm</i>)	1E	00011110	30	
16	Max V image size (<i>rounded to cm</i>)	13	00010011	19	
17	Display Gamma (<i>=(gamma*100)-100</i>)	78	01111000	120	
18	Feature support (<i>no DPMS, Active OFF, RGB, tmg Blk#1</i>)	0A	00001010	10	
19	Red/green low bits (Lower 2:2:2:2 bits)	7F	01111111	127	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	E5	11100101	229	
1B	Red x (Upper 8 bits)	93	10010011	147	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	50	01010000	80	
1E	Green y	8C	10001100	140	
1F	Blue x	27	00100111	39	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	



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35		01	00000001	1	
36	Pixel Clock/10000 LSB	C7	11000111	199	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active Lower 8bits	00	00000000	0	
39	Horz blanking Lower 8bits	A0	10100000	160	
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	01010000	80	
3B	Vertical Active Lower 8bits	20	00100000	32	
3C	Vertical Blanking Lower 8bits	17	00010111	23	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	36	00110110	54	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	2F	00101111	47	
43	Vertical Image Size Lower 8bits	BD	10111101	189	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border (<i>zero for internal LCD</i>)	00	00000000	0	
46	Vertical Border (<i>zero for internal LCD</i>)	00	00000000	0	
47	Signal (<i>non-intr, norm, no stero, sep sync, neg pol</i>)	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	



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70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	34	00110100	52	4
74	Manufacture P/N	31	00110001	49	1
75	Manufacture P/N	45	01000101	69	E
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	35	00110101	53	5
79	Manufacture P/N	20	00100000	32	
7A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	31	00110001	49	1
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	97	10010111	151	
			SUM	6144	
			SUM to HEX	1800	